

REAL-TIME UNDERLOAD TAP-CHANGER CONTROL BASED ON SYNCHROPHASOR MEASUREMENTS

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This paper proposes a new system integrity protection scheme algorithm using transformer under-load tap changer control based on wide area synchrophasor measurements in order to prevent further degradation of the bus voltages in the power system. The impact of various trigger-types on the voltage stability of the power system is investigated. A wide area monitoring, protection, and control “proof-of-concept” testbed is implemented using the real-time digital simulator in combination with industrial-grade equipment comprising of phasor measurement units, phasor data concentrators, programmable logic controller, and communication network switches. The proposed algorithm is tested and validated using an equivalent 10-bus multi-machine test system, and the results obtained verifies its effectiveness.

1. INTRODUCTION

As system loading increases and the power system is stressed beyond its design limits, voltage instability and voltage collapse is inevitable. Therefore, it is necessary to have in place system integrity protection schemes (SIPS) to preserve the integrity of the power system after a disturbance by preventing power system instability before it becomes system-wide [1, 2].

The IEEE Power System Relaying Committee (PSRC) Working Group C4 Report of October 2010 on “Global Industry Experiences with System Integrity Protection Schemes” [2] identified a couple of remedial actions for mitigating power system instability. Some of the corrective actions that can be applied in mitigating voltage collapse in particular include shunt capacitor switching [3], load shedding [4–6], and tap-changer control [6–10]. A system can be driven to voltage collapse through system faults, line/generator contingencies, the action of transformer under-load tap changers (ULTCs), operation of generator over-excitation limiters (OXL), increased loading, and the load recovery characteristics at low voltages [1, 11, 12]. In order to prevent further degradation of the system voltages, transformer ULTC control is a remedial action that can be used to halt and prevent further taps of the transformer ULTC. Tap-changer control using voltage thresholds as control parameters was proposed in [6–10]. However, this results to control actions being initiated prematurely without giving the system time to recover.

This paper presents a SIPS algorithm using transformer ULTC blocking and unblocking (ULTC-SIPS) for preventing power system voltage instability and voltage collapse using wide area synchrophasor measurements obtained from phasor measurement units (PMUs). The ULTC-SIPS control actions are implemented using the IEC 61850 Generic Object Oriented Substation Event (GOOSE) messages. Also, a real-time voltage stability assessment (RVSA) index [12] is applied in the prediction of the system operating state, and is used as one of the inputs to the arming trigger of the proposed ULTC-SIPS control algorithm, rather than voltage thresholds as found in the existing literature. Furthermore, a “proof-of-concept” testbed was developed

to test the proposed ULTC-SIPS algorithm in real-time using hardware-in-the-loop simulations.

The rest of this paper is organized as follows: Section 2 gives an overview of the proposed ULTC-SIPS algorithm and its functional elements. Section 3 presents the real-time lab-scale “proof-of-concept” testbed used in the implementation and validation of the proposed algorithm. The simulation results obtained are presented and discussed in Section 4.

2. OVERVIEW OF THE PROPOSED ALGORITHM

Power system protection is a very important aspect of the electric power system. However, most protection devices are designed for the local protection of specific equipment like generators, transformers, transmission lines, buses, and feeders. Such protection devices are not capable of providing effective system security for system-wide conditions. System-wide conditions are better protected using SIPS. SIPS are designed to detect abnormal system conditions and implement predetermined remedial actions to preserve the integrity of the power system [2, 13]. They can be classified into the following categories [13]: (i) centralized and decentralized SIPS; (ii) event-based and response-based SIPS; (iii) rule-based and algorithmic-based SIPS; and (iv) closed-loop and open-loop SIPS. Generally, the components of SIPS can be divided into three main functional elements [14]. These include: (1) system monitoring element; (ii) protection element; and (3) control execution element.

The proposed SIPS implemented in this paper uses a transformer ULTC blocking and unblocking algorithm designed to control the tap action of the transformer ULTC. The three functional elements mentioned above are implemented in the SIPS algorithm as shown in Fig. 1. The system monitoring element is applied in the supervision and detection of the changes in the power system. These changes can be in the system topology, the load demand, and the generation output. The inputs to the system monitoring element include: (i) system operating status; (ii) key generator OXL status; and (iii) load bus voltage deviation.

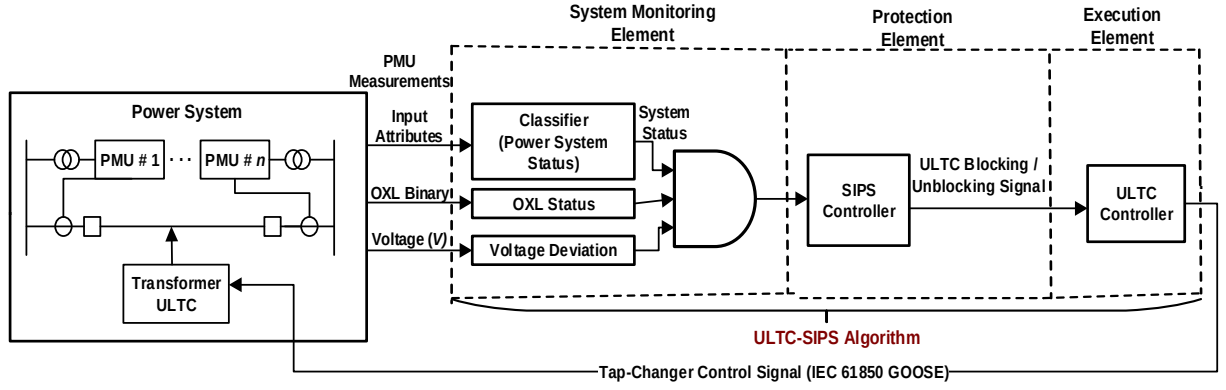


Fig. 1 – Block diagram of the functional elements of the proposed ULTC-SIPS algorithm.

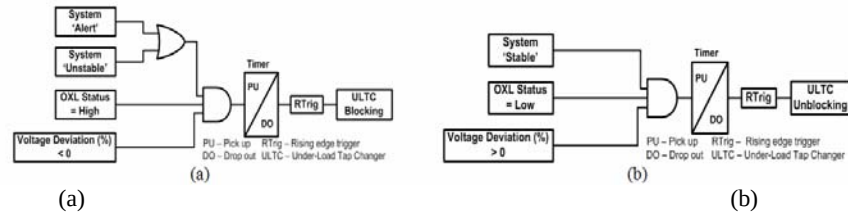


Fig. 2 – ULTC-SIPS algorithm a) blocking signal; b) unblocking signal.

The generators in a power system can be grouped into reactive power reserve basins (RPRBs) [15–17] comprising of generators providing reactive power support to each voltage control area (VCA) in the power system. The key generator in the RPRBs can be used to provide an indication of the system's margin to voltage collapse, and can be subsequently applied in the prediction of the system's operating state [12, 18].

A real-time voltage stability assessment (RVSA) index based on the effective generator field current reserve (EGFCR) available on the key generator was proposed by the authors [12, 18]. The RVSA index gives the system's margin to voltage collapse, and it is given as [12, 18]:

$$RVSA_{Ifd} = \left(\frac{I_{fd \max}^c - I_{fdk}}{I_{fd \max}^c} \right) \times 100\%, \quad (1)$$

$$RVSA_{Ifd} = \left(1 - \frac{I_{fdk}}{I_{fd \max}^c} \right) \times 100\%, \quad (2)$$

where I_{fdk} is the field current at the k th operating time, $I_{fd \max}^c$ is the maximum field current at the point of voltage collapse.

A decision tree (DT)-classifier [12] is developed and trained to predict the status of the power system based on the $RVSA_{Ifd}$ index [12] obtained for various system operating conditions and credible contingencies. In this paper, wide area measurements from PMUs are used as the inputs to the SIPS. The output of a DT-classifier [12] predicting the system operating state ("Stable", "Alert", or "Unstable") serves as one of the inputs (trigger) to the system protection element of the ULTC-SIPS algorithm instead of a fixed voltage threshold. Unlike voltage

thresholds, the use of the system status information makes the proposed algorithm robust, as it is able to respond to various system dynamics as the power system condition changes. The other inputs to the system protection element include the voltage deviation of the bus connected to the regulated side of the transformer computed using PMU positive sequence voltage phasor (V_1), the OXL of the key generator using PMU analogue measurements, and the pick-up time delays. The pick-up time used in this paper for the blocking signal is 0.5 s, while the pick-up time for the unblocking signal is 5 s. Figure 2a shows the logic used in blocking the transformer ULTC taps during stressed conditions, while Fig. 2b is for unblocking the ULTC after the system recovers. The protection element is applied in the identification of system stability threats and the arming of the SIPS to mitigate such stability threats. Five trigger-types were investigated respectively. The execution element receives the output signal from the protection element and performs the required remedial action.

In the proposed algorithm, the ULTC blocking signal is transmitted using a 'remote bit set' signal from the SEL-3378 synchrophasor vector processor (SVP) to the ULTC controller modelled in the RSCAD software, while the unblocking signal to the transformer ULTC controller is transmitted using a "remote bit clear" signal. The parameters used in the modelling of the ULTC are given in [1, 12]. The procedure involved in the SIPS implementation is shown in Fig. 3. This comprises of an offline process where the DT-classifier is grown using various operating conditions/credible contingencies to predict the system state, an online process involving the deployment of the grown DT-classifier in the SEL-3378 SVP, and the real-time testing of the SIPS algorithm as illustrated in Fig. 3. More information on this can be found in [12].

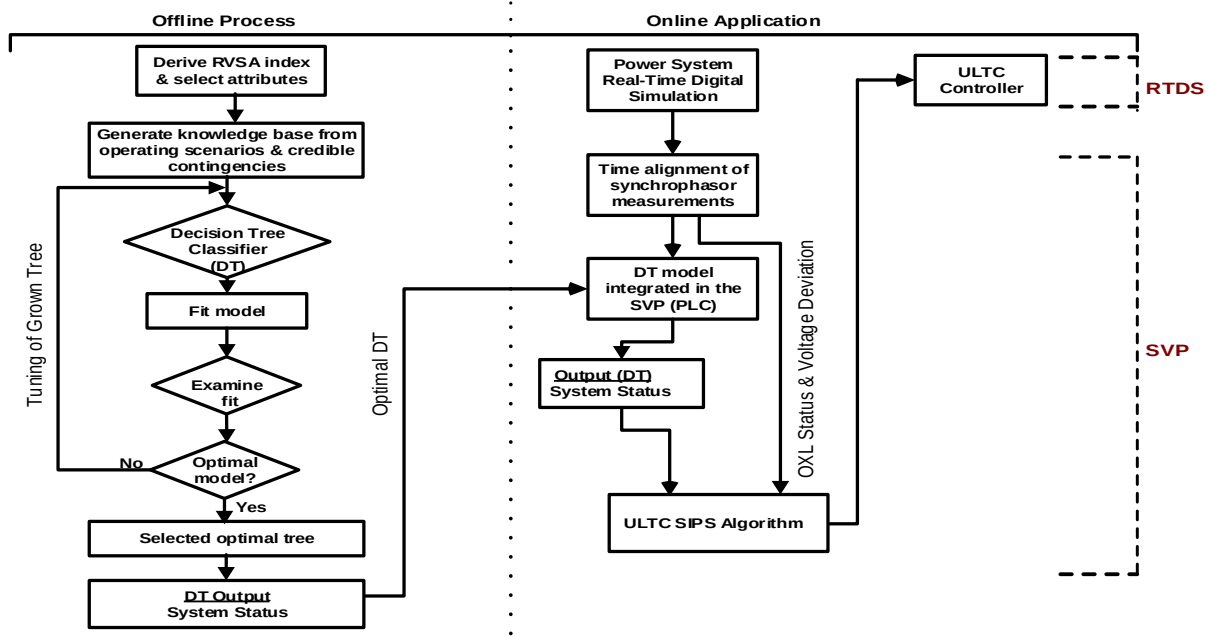


Fig. 3 – Implementation of the ULTC-SIPS algorithm.

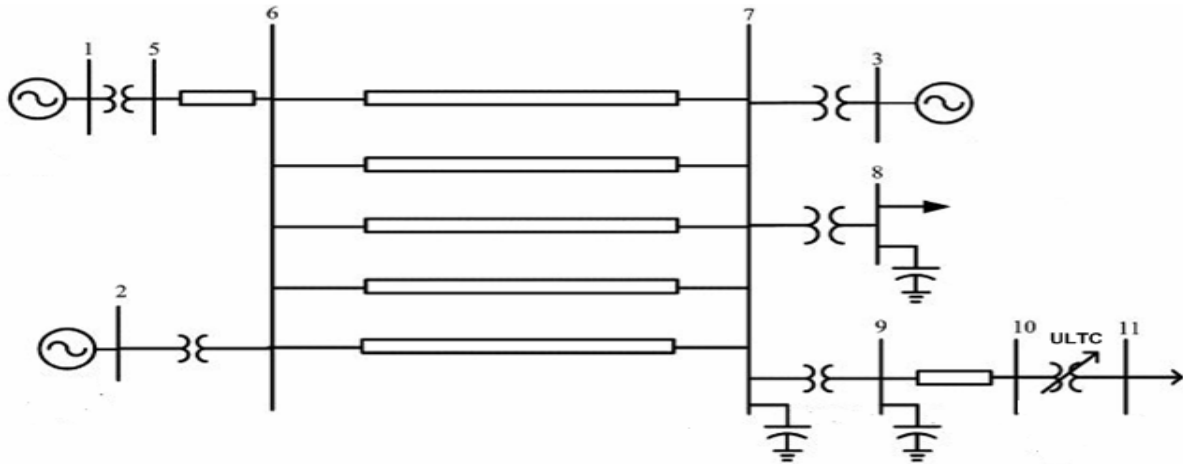


Fig. 4 – 10-bus multi-machine study network [1].

3. REAL-TIME LAB-SCALE IMPLEMENTATION

3.1. STUDY NETWORK MODELLING

The testing and validation of the proposed SIPS algorithm was carried out using a 10-bus multi-machine network [1, 12] shown in Fig. 4. This was modelled using the RSCAD software. The study network is made up of three generators supplying a total of 6,655 MW of load at load level-1, with generators G1 and G2 injecting a total of 5,717 MW across five 200 km, 500 kV transmission lines. Generator G3 supplies the rest of the power required, and it is located at the load centre.

A transformer ULTC is incorporated between buses 10 and 11. When the bus voltage p.u. at bus 11 rises or drops below the regulated voltage threshold (0.95 p.u.), the ULTC taps up or down. Further information on the modelling of the study network and the parameters used can be found in [1, 12].

3.2. TEST PLATFORM

The “proof-of-concept” testbed developed in this paper comprises of the real-time digital simulator (RTDS®) incorporating the giga transceiver network (GTNET) protocol comprising of GTNET-PMU and GTNET-GSE protocols, external PMU hardware, phasor data concentrator (PDC), SEL-3378 SVP, GPS satellite clock, and industrial communication network switches [12]. The RTDS® is used in the simulation of the study network modelled in RSCAD software, and the simulations are carried out in real-time with a time-step of 50 microseconds. The GTNET-PMU and the external PMUs transmit the IEEE C37.118 synchrophasor measurements onto the communication network. Some parameters that need to be configured include the station name, configuration frame format, PMU identification (PMU ID), reporting rate, port number, phasor formats, phasor output format, number of phasors, number of analogues values/digital word.

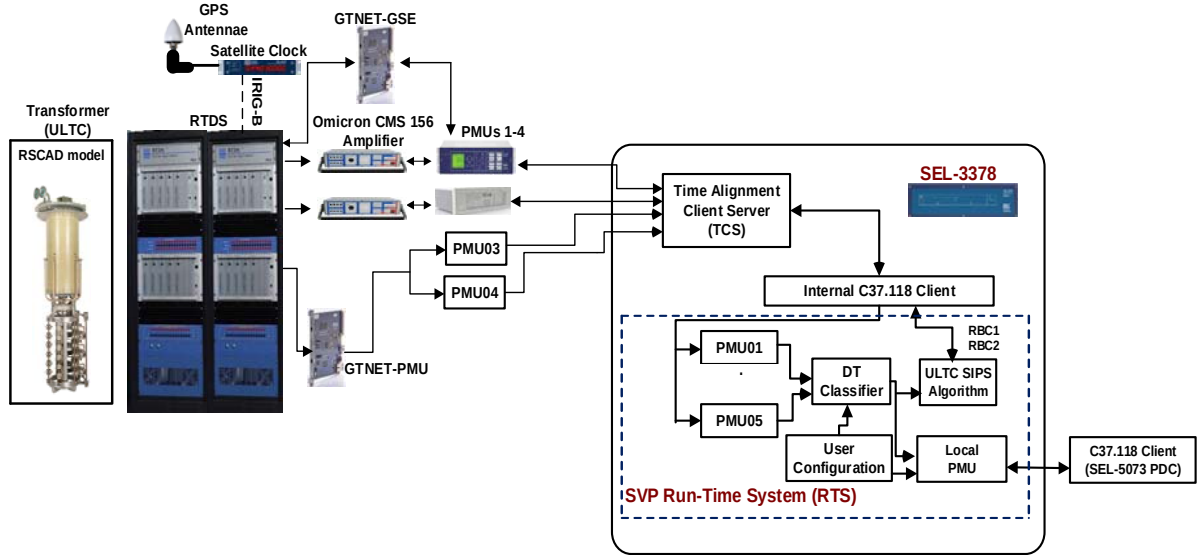


Fig. 5 – Lab-scale set-up of the ULTC-SIPS algorithm.

The SEL-3378 SVP was configured as a PDC and also as a programmable logic controller (PLC). The system monitoring and protection elements of the proposed ULTC-SIPS algorithm, and the DT-classifier [12] previously trained in MATLAB are integrated/programmed in the SEL-3378 SVP using the IEC 61131-3 structured text (ST) codes. The layout of the lab-scale testbed is shown in Fig. 5.

The time alignment client server (TCS) shown in Fig. 5 carries out the time-alignment of the synchrophasor measurements from the PMUs. The aligned measurements from the TCS are interfaced to the run-time system (RTS) via the internal IEEE C37.118 Client shown in Fig. 5. The local PMU shown in Fig. 5 is an internal IEEE C37.118 Server used in publishing the output datastream of the SEL-3378 SVP to external IEEE C37.118 clients (e.g. PDCs).

The various components of the system monitoring element comprising of the system operating status [12], OXL status of the key generator, and the voltage deviation calculation were implemented using IEC 61131-3 ST codes. Similarly, the protection element is implemented in the SEL-3378 SVP using ST codes. The execution element transmits a fast operate (FO) command (RBC1/RBC2) from the SEL-3378 SVP port to the telnet port of the SEL-451 intelligent electronic device (IED) which serves as a PMU and also as the actuator module to the transformer ULTC controller modelled in the RSCAD software. The FO command received by the SEL-451 IED is published as an IEC 61850 GOOSE message to the transformer ULTC controller via the RTDS GNET-GSE card.

3.3. SIMULATIONS

Data from real-time simulations was used in building the knowledge base for training the DT-classifier [12]. A total of 504 observations obtained from various operating scenarios including transmission line contingencies, increased system loading, ULTC tap action, and generator OXL operation were used in generating the dataset required for training and testing the DT-classifier [12]. The input of the learning set (LS) comprises of PMU measurements of the positive sequence voltage phasor (V_1) at buses 7, 8, 10, 11, bus voltage phase angle difference, real and reactive powers

from generator G3, and field current from G3. The output of the DT-classifier is a discrete response with three classes (“Stable”, “Alert”, and “Unstable”). Further information on the DT-classifier used can be found in [12, 18].

The system loading involves a percentage increment in real and reactive powers every 60 s at a constant power factor. MATLAB 7.12.0 (2011a) and MATLAB Statistics Toolbox are used in the design (growing) of the DT-classifier [12]. 70 % of the observations were used as the LS, while the remaining 30 % were used as the test set (TS) for the validation of the trained DT-classifier. The DT-classifier has a discrete output of “Stable”, “Alert”, and “Unstable” signifying the system’s operating state.

4. RESULTS AND DISCUSSION

Figure 6 shows a voltage collapse scenario for a case study involving increased system loading at bus 8, loss of one of the transmission lines between buses 6 and 7, transformer ULTC action, and generator G3 OXL operation. In order to implement the proposed ULTC-SIPS algorithm, a comparison was carried out using various trigger-types (SIPS protection element). Fig. 7 shows the plot of trigger-type 1 which is commonly used, and trigger-type 5 which is proposed in this paper. The SIPS trip time is calculated from the start of the system disturbance to when the protection element of the SIPS algorithm (trigger) was armed.

From Fig. 6, it can be seen that a voltage collapse occurred with the voltage at bus-10 equal to 0.6663 p.u., while the voltage at bus-11 was 0.722 p.u. Table 1 presents the average SIPS trip time for all the SIPS trigger-types considered. From Table 1, it can be seen that the fastest trip time was obtained using trigger-type 1. However, it can be seen from Table 2 that the voltage levels were still high at the time of operation of the SIPS trigger-type 1. Fig. 8 shows a case study simulated using a loss of line contingency without and with the proposed ULTC-SIPS algorithm using trigger-type 5. The ULTC-SIPS algorithm was used to block further taps of the ULTC before the onset of voltage collapse.

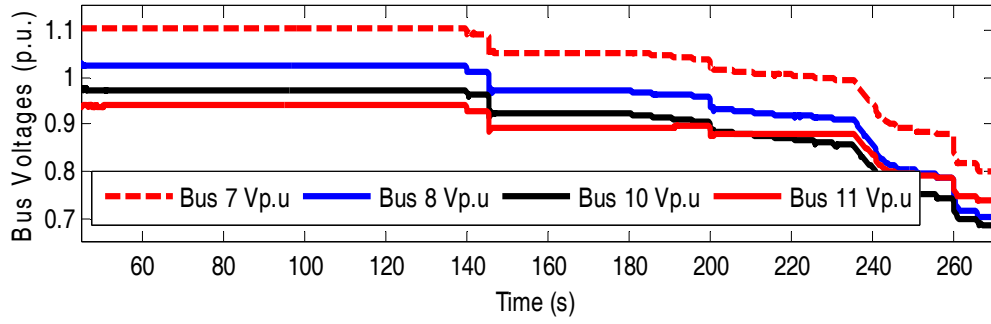


Fig. 6 – Voltage plots for buses –7, –8, –10, and –11.

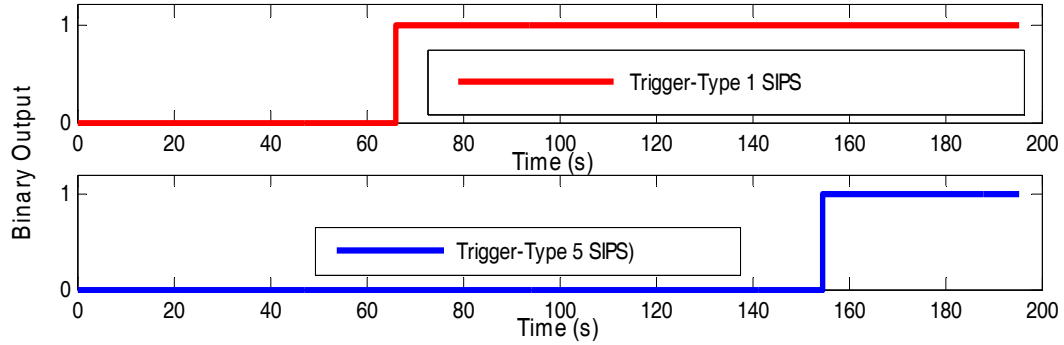


Fig. 7 – Plots of trigger-type 1 and trigger-type 5 for the proposed ULTC-SIPS algorithm.

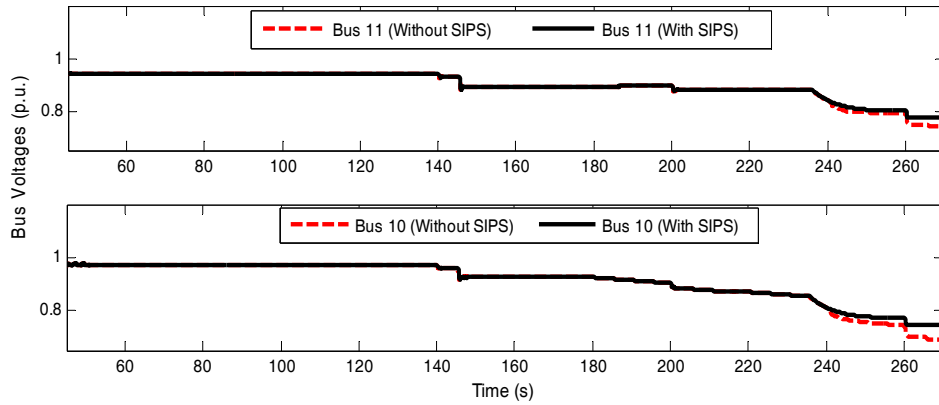


Fig. 8 – Voltage plots for buses –10 and –11, with and without the proposed ULTC-SIPS algorithm.

Table 1

Average trip time for various trigger-types

Trigger No.	Trigger-type	Time (s)
1	Voltage threshold only	66.15
2	OXL status only	156.10
3	System status only	120.60
4	Voltage threshold and OXL status	156.00
5	System status, voltage threshold, and OXL status	156.20

Table 2

Bus voltages for various trigger-types and test cases without ULTC-SIPS algorithm

Trigger	Bus voltages p.u. (With SIPS)				Bus voltages p.u. (Without SIPS)	
	Bus 7	Bus 8	Bus 10	Bus 11	Bus 10	Bus 11
1	1.0116	0.9250	0.8863	0.8541	0.6663	0.7222
2	0.8679	0.7740	0.7458	0.7726		
3	0.9963	0.9092	0.8671	0.8564		
4	0.8679	0.7740	0.7458	0.7726		
5	0.8679	0.7740	0.7458	0.7726		

Voltage collapse was avoided with the voltage at bus-10 settling at 0.7458 p.u., while the voltage at bus-11 settled at 0.7726 p.u. From the results obtained above, it can be seen that trigger-type 1 based on voltage threshold operated prematurely without giving the system time to recover.

Good operate time with an acceptable voltage level was obtained using trigger-type 3 (in bold). However, for the power system considered, simulations carried out show that trigger-type 5 fits better and demonstrated consistency for the various simulation scenarios carried out when compared with the other four trigger-types.

5. CONCLUSION

This paper presents a transformer ULTC blocking/unblocking SIPS (ULTC-SIPS) algorithm using inputs based on synchrophasor measurements, and control signals using IEC 61850 GOOSE messages. The inputs to the protection element of the ULTC-SIPS algorithm are the output of a DT-classifier (system operating state), voltage deviation at the low voltage side of the transformer, and the status of the key generator OXL. Also, an investigation on various trigger-types was carried out. Trigger-type 5 is proposed in this paper because it demonstrated robustness and did not operate prematurely like trigger-type 1. Thus, it was able to respond to various system dynamics involving a wide range of system disturbance levels.

Furthermore, the SIPS algorithm was deployed in the PLC (SEL-3378 SVP) for real-time hardware-in-the-loop testing with the RTDS[®]. Results obtained showed that voltage collapse can be mitigated if the ULTC tap action is timely blocked before the system becomes unstable. The proposed algorithm was shown to be an efficient remedial action for providing temporary relief in the prevention of further degradation of the system voltages.

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