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RESEARCH ARTICLE

Design and Analysis of On-Chip Reconfigurable SCVR With Wide Output Voltage Range for SoCs

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ABSTRACT A comprehensive framework for the analysis and design of reconfigurable two-phase switched-capacitor (SC) dc-dc converters is introduced. Initially, a generalized approach leveraging graph theory and network analysis is presented, enabling the enumeration of all possible ideal conversion ratios for a given SC converter topology. This methodology extends the performance boundaries of two-phase SC converters, leading to the proposal of a reconfigurable, two-phase SC dc-dc converter. The proposed converter incorporates a programmable, optimized switching configuration that enhances the number of achievable ideal conversion ratios for a fixed set of capacitors and switching states. This flexibility enables the converter to operate with high efficiency across a broad spectrum of operating conditions while achieving significantly high step-down conversion ratios. This work presents a reconfigurable, fully integrated, two-phase interleaved switched-capacitor voltage regulator (SCVR) with an on-die MIM capacitor intended for low-power system-on-chips (SoCs). High power density and efficiency are made possible in on-chip switched-capacitor (SC) converter implementations using MIM capacitors with a low bottom-plate parasitic. The charge-multiplier model for reconfigurable SCVR is investigated and verified through modeling and simulation. With varying power supplies of 1.24 V, 1.15 V, and 1.03 V, a reconfigurable SCVR having four voltage conversion ratios (VCRs) has been designed to provide dynamic voltage scaling (DVS) of many-core microprocessors on a per-core basis. Further, the converter's parasitic and charge-sharing losses are efficiently reduced by utilizing switch and frequency scaling techniques. The proposed SCVR is reconfigured into four gain topologies having VCRs 5:4, 4:3, 3:2, and 1:1 respectively. The nominal output voltage of the converter ranges from 0.6 V to 1 V, from three different power supplies. The proposed converter has a maximum load current of 625 mA and a peak efficiency of 81.09%. Further, it delivers load current ranging from 200 mA to 625 mA with an efficiency greater than 70%. To validate the design, it is developed and simulated using a 22 nm CMOS process. MATLAB and PSpice simulation tools are used to verify the results.

INDEX TERMS Dc-dc converter, power management, reconfigurable SCVR, series-parallel, switched-capacitor.

I. INTRODUCTION

System-on-chip (SoC) technology, which integrates different components of an electronic system onto a single chip, has emerged as the most promising approach for maximizing chip area utilization and reducing power consumption during the last ten years. Complex very large-scale integration (VLSI) circuits and systems require properly managed fully integrated voltage control since different components per core require different supply voltages and it is necessary to adjust these voltages rapidly. Therefore, on-chip power management units (PMU) must incorporate highly efficient fully integrated DC-DC converters, as the computing units are switching to many-core architecture. Switched-capacitor (SC) based voltage regulators are considered to be the most promising on-chip voltage control technology. They have increasingly demonstrated their benefits by attaining high conversion efficiency and producing many on-chip supply

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domains with few shared supply pins [l]. In recent times, interest in monolithic power conversion for SC DC-DC converters has grown quickly. Compared to inductor-based switched-mode converters, these converters efficiently eliminate IR drop and provide efficient power conversion since they do not experience the substantial degradation of power delivery network (PDN) impedance that can arise with additional off-chip supply [2], [3], [4].

As the number of cores increases, there is a growing demand for using a separate power supply for each core and functional block to maximize total chip power and performance, as shown in Fig. 1. A single switching regulator in the first stage of the distributed power delivery network (PDN) reduces the primary supply voltage to an intermediate level, and a variety of second-stage switching regulators provides the core voltage. With just one external SC converter used in this configuration (Fig. 1), the circuit complexity and motherboard area for the PDN are greatly reduced. Consequently, there is a 3-4% improvement in voltage regulation efficiency [5]. The overall efficiency and performance would suffer more if additional off-chip SC converters were added as the power supply impedance would rise dramatically. As a result of this reduction, sub-threshold and gate leakage power decline more than linearly, while dynamic switching power decreases substantially. Voltage conversion is therefore becoming more and more important as performance and power requirements tighten in both low-power applications such as SoCs and traditional microprocessors. To address these issues, on-chip voltage regulators have evolved into a crucial component of PMU. Hence, the voltage regulator is integrated into the chip to reduce conduction and parasitic losses in PDN. Transistors and capacitors are the only components of SC-based converters. Due to the simplicity of capacitor and transistor on-chip integration, the SCVR is regarded as one of the most promising options [6], [7].

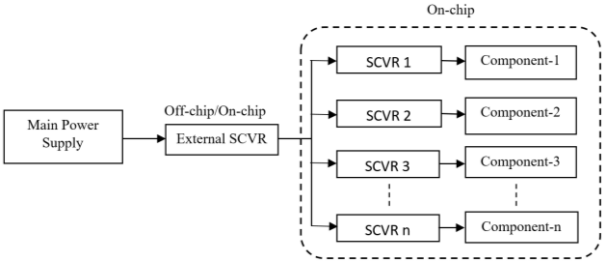


FIGURE 1. PDN features on-chip SC converters along with a single on/off-chip SC converter.

Generally, the best power-cell capacitor sizing with optimal capacitance utilization may be accomplished with SC converter designs having single-VCR. However, limited VCRs and confined efficiency optimization over a small range are typical issues with these converters. To overcome these concerns, fine-grained reconfigurable SCVRs have been introduced, boosting efficiency throughout a broader VCR range to handle variable input and output voltages. Power cell partitioning and reconfiguration enable numerous VCRs with this reconfigurable architecture, which is essential for the overall optimization of PCE. It also permits full capacitance use and ideal power-cell dimensions under each conversion ratio.

However, various factors such as the bottom plate capacitance, the transistor's conduction and switching losses, their parasitic capacitances and the VCRs limit SCVR performance [8], [9]. Due to these restrictions, it is difficult to acquire the appropriate voltage level, efficiency, and power density as well as the load current required by the chip. Due to these constraints, it is difficult to satisfy the required specifications for load current, efficiency, power density, and voltage levels. Various designs of SC converters have been put forth to address these issues. Several design goals, such as dynamic voltage scaling (DVS), variable VCRs, high efficiency, and high power density, are highly demanded for SCVR. These objectives present additional challenges to the robustness of the system. It has been demonstrated that increasing power density and improving efficiency can be achieved by implementing new feed-forward control strategies in conjunction with a selection of capacitor types to reduce bottom-plate capacitance losses [10], [11], [12]. In general, the charge sharing, conduction and switching losses typically limit the efficiency of SCVR. The efficiency is also greatly impacted by parasitic losses in addition to these other considerations. Recent research has demonstrated that, for power levels up to 1W, the use of different types of integrated capacitors, such as trench capacitors, metal-oxide-semiconductor (MOS) and stacking metal-insulator-metal (MIM) capacitors can achieve performance comparable to the linear converter. Therefore, creating a topology that is both reliable and power-efficient is essential, particularly for multiphase converters. However, standard SC converters are inefficient for DVS systems as they only attain high efficiency at their ideal VCR. This constraint can be addressed with an SC converter containing multiple reconfigurable VCRs. A two-phase interleaved reconfigurable SCVR that offers a range of conversion ratios designed for high power efficiency for SoCs is proposed in this work. In addition, the suggested on-die high-density MIM capacitor can successfully lower the converter's parasitic and charge-sharing losses by combining switch and frequency scaling techniques. To address the aforementioned issues, this paper investigates a steady-state charge-multiplier model of two-phase interleaved reconfigurable SCVR providing four different VCRs under varying supply voltages of 1.03 V, 1.15 V and 1.24 V. To enhance efficiency, the fundamental SC converter analysis is modified to develop formulations for the minimum power loss by taking into account the effects of conduction, switching, and parasitic loss. The suggested model has been verified with PSpice simulation. To reduce parasitic and charge-sharing losses while ensuring simple circuit implementation, an on-die MIM capacitor with a low equivalent series resistance (ESR) and high capacitance density is introduced. This work discusses features of the design and implementation of reconfigurable SCVR within

a broad range of input/output voltages and load currents. The paper is organized as follows: A steady-state charge multiplier model of SCVR is introduced in Section II. Key circuit blocks and the proposed two-phase interleaved SCVR, featuring a low-parasitic on-die MIM capacitor are discussed in Section III. Section IV describes optimization strategies that enable the efficient use of switch size and switching frequency for enhanced power efficiency for a given output impedance. Simulation results of reconfigurable SCVR designed for 200mA to 625mA load current implemented in 22nm tri-gate CMOS process are presented in Section V. Finally, conclusion is provided in Section VI.

II. CHARGE-MULTIPLIER MODEL: STEADY-STATE ANALYSIS

SC DC-DC converters have several advantages over inductive ones, including the ability to scale to desired power levels and ease of on-chip integration. This makes them a potential option for integrated voltage regulators, particularly for compact, low-power devices. The output equivalent resistance (R_{eq}) is a key performance metric used to evaluate and contrast various SC converters. A steady-state model with an ideal DC transformer with a turns ratio n which depends on the circuit topology followed by R_{eq} is obtained by circuit averaging of SC DC-DC converters, as shown in Fig. 2 [13]. The steady-state model of SCVR also consists of a resistor R_p that models the parasitic loss whereas R_{eq} models the charge sharing loss. This model provides a clear link between topology, efficiency, and overall device area [14]. For SC converters, the R_{eq} is an essential parameter since it has a fundamental impact on the converter's steady-state performance, which includes efficiency and load regulation. The introduction of ''charge multipliers,'' a powerful concept that aids in estimating component peak, average, or RMS current ratings in addition to finding R_{eq} Charge multipliers are governed by circuit topology and are derived using basic principles of network theory [15], [16].

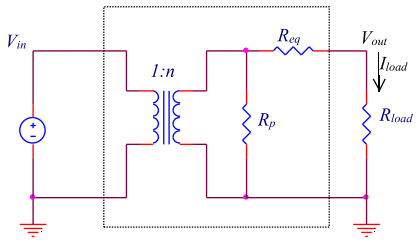


FIGURE 2. Steady-state model of SCVR.

Topology generation is the primary concern for the majority of converter designs. The five common topologies employed by SC-based DC-DC converters are Dickson, Fibonacci, Doubler, Ladder, and Series-Parallel (SP). The SP architecture is the most efficient in terms of capacitor use among them all [17]. Furthermore, the performance of various converter topologies is assessed and contrasted using two essential metrics namely Slow-Switching-Limit (SSL) and Fast-Switching-Limit (FSL) impedances [18], [19]. When the resistances of the switches, capacitors, and connecting lines predominate, the converter operates in the FSL region, with the capacitors acting as fixed voltage sources. Further, the current flows in a piecewise constant pattern irrespective of switching frequency. On the other hand, with the SSL region, the switching frequency and impedance are inversely related. A sequence of charge-multiplier vectors defines these regions of operation. The ratio of the total charge delivered throughout a full switching period (T_s) to the charge flowing through each component is known as a charge multiplier.

Further, the theoretical efficiency of an SCVR is $\eta = V_o/(nV_i)$, where n is the optimal VCR. The SSL impedance is calculated under the assumption that the switches, and capacitors are ideal and interconnect lines have minimal finite resistance. The SSL impedance is given as

$$R_{ssl} = -\frac{V_{out}}{I_{out}} = \frac{1}{f_{sw}} \sum_i \frac{(a_{c,i})^2}{C_{flyi}} \tag{1}$$

In equation (1) the capacitance of an i^{th} flying capacitor is denoted by C_{flyi}, $a_{c,i}$ represents the i^{th} value of the charge-multiplier vector (a_c) and f_{sw} is the switching frequency. The duty cycle of the converter is assumed as 50% and hence the load draws the same amount of current in both phases. However, the capacitor never reaches an equilibrium state at high fsw [20]. Therefore, on-state switch and interconnect impedances are the main causes of FSL loss. S The duty cycle in the case of FSL impedance is crucial since the converter current flows continuously during the switching cycle. Additionally, it is assumed that the voltage and current across the capacitors are almost constant, and that the power loss is caused by conduction loss rather than the ripple voltage loss of the capacitors [21]. The FSL impedance is calculated as

$$R_{fsl} = 2 \sum_i R_{on,i} (a_{r,i})^2 \tag{2}$$

In equation (2), the variable R_{on} is the switch on-resistance of the unit cell and $a_{r,i}$ is the charge-multiplier vector of i^{th} switch. An SCVR overall output impedance is comprised of both FSL and SSL impedances. As these impedances are estimated under various operating conditions, they cannot be added directly. The optimal operating point should be selected at the knee point within SSL and FSL regions. Since R_{eq} is difficult to formulate precisely, many converters use the quadratic sum approximation [22], given as

$$R_{eq} \approx \sqrt{R_{ssl}^2 + R_{fsl}^2} \tag{3}$$

III. CIRCUIT IMPLEMENTATION

Generally, there are two types of reconfigurable SCVRs. As mentioned in [8], [10], and [11], the first type is called ''direct reconfigurable'' and comprises SP converters. The SC converter that is proposed in this work also uses direct reconfiguration. Cascaded reconfigurations are included in the second category. SC converters appear to be less

suited for DVS applications due to their intrinsic conduction losses, which can lower energy efficiency. Further, the limited number of conversion ratios offered by many SC DC-DC converters prevents them from being used in systems where either the input voltage or the output voltage varies. Reconfigurable SCVR with numerous peaks of efficiency are employed to get around this [13]. To do this, multiple intermediate VCRs are used. This is crucial for wireless systems since battery voltage steadily decreases in these systems. To overcome the efficiency constraints of a single topology, this work introduces an SC step-down DC-DC converter that modifies its open-loop topology into multiple VCRs according to the input voltage.

A. PROPOSED RECONFIGURABLE SCVR

The circuit's design configuration largely determines how the SCVR operates, with the flying capacitor ratio being a key factor in voltage regulation. The capacitor array's internal charge redistribution allows for voltage conversion. Initially, the capacitors are charged in the first phase, and then in the second phase, they are discharged to the load. During these two phases, the network topology determines the VCR. The proposed converter is based on a two-phase interleaved reconfigurable SC architecture. Reconfigurable architecture with a range of topologies is used in SC DC-DC converters designed to operate with varying input or output voltages [23] to assure high efficiency under different operating conditions. The proposed reconfigurable SCVR, shown in Fig. 3, has four distinct gain settings that are used to adjust the output voltage: 5:4, 4:3, 3:2, and 1:1, as represented in Fig. 4 (a)-(d). Because of its modular architecture, this voltage regulation solution is both efficient and compact, making it appropriate for a wide range of applications. The primary components of the SC core are 17 switches, as shown in Fig. 4(e), which are driven by clock signals φ_1 and φ_2.

Additionally, an NMOS transistor is used for the implementation of a switch that has a terminal linked to either the ground or the output voltage. Instead, a switch implementation using a PMOS would need to produce a negative supply. The core consists of four charge transfer capacitors C_1–C_4, 0.4nF each. The entire capacitance is divided equally among four capacitors to maximize on-chip capacitance for various configurations. As shown in Table 1, the 1.24 V, 1.15 V, and 1.03 V supply voltages are transformed into a regulated load voltage during operation. With this arrangement, performance and stability are increased across a range of voltage levels, ensuring that the output remains consistent regardless of the varying input conditions.

1) MIM CAPACITOR TILE STRUCTURE

Capacitor area and performance are important parameters in fully integrated SC converter implementations in CMOS technologies. Another important consideration in the design of a SC converter is the capacitance density of the flying capacitors. The SP topology stands out as the most efficient solution for capacitance utilization due to its beneficial design. The selected capacitor technology has a major impact on efficiency and space usage, which in turn affects the performance of SC converters.

Metal-oxide-metal (MOM), Metal-insulator-metal (MIM), Deep-Trench, and MOS capacitors are examples of common capacitor technology. Every technology has unique features and structural properties that determine how well it performs and is suitable for various applications [24], [25]. The flying capacitors are implemented as MIM capacitors, which are considered the most suitable selection for fully integrated circuits because they offer a much lower bottom plate capacitance and are also available in regular CMOS. A MIM capacitor of 0.4nF is taken into account for each flying capacitor yielding a total capacitance of 1.6nF, as shown in Table 2. An input voltage of 1.24V is considered. Switch and pre-driver parasitics are included in the extracted netlist of the MIM capacitor, which is utilized for conducting PSpice simulations. The MIM tile structure's frequency response is shown in Fig. 5. Additionally, the ESR value for 1.6nF capacitance (@ 100MHz) is 0.5 Ω, with four MIM tiles supported per core.

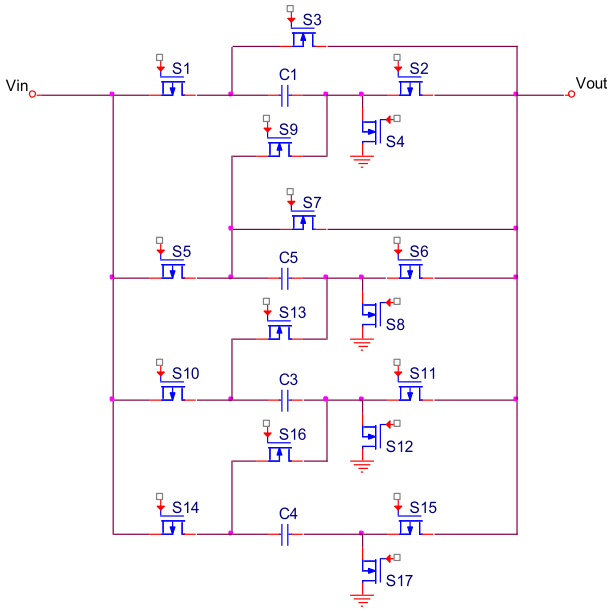
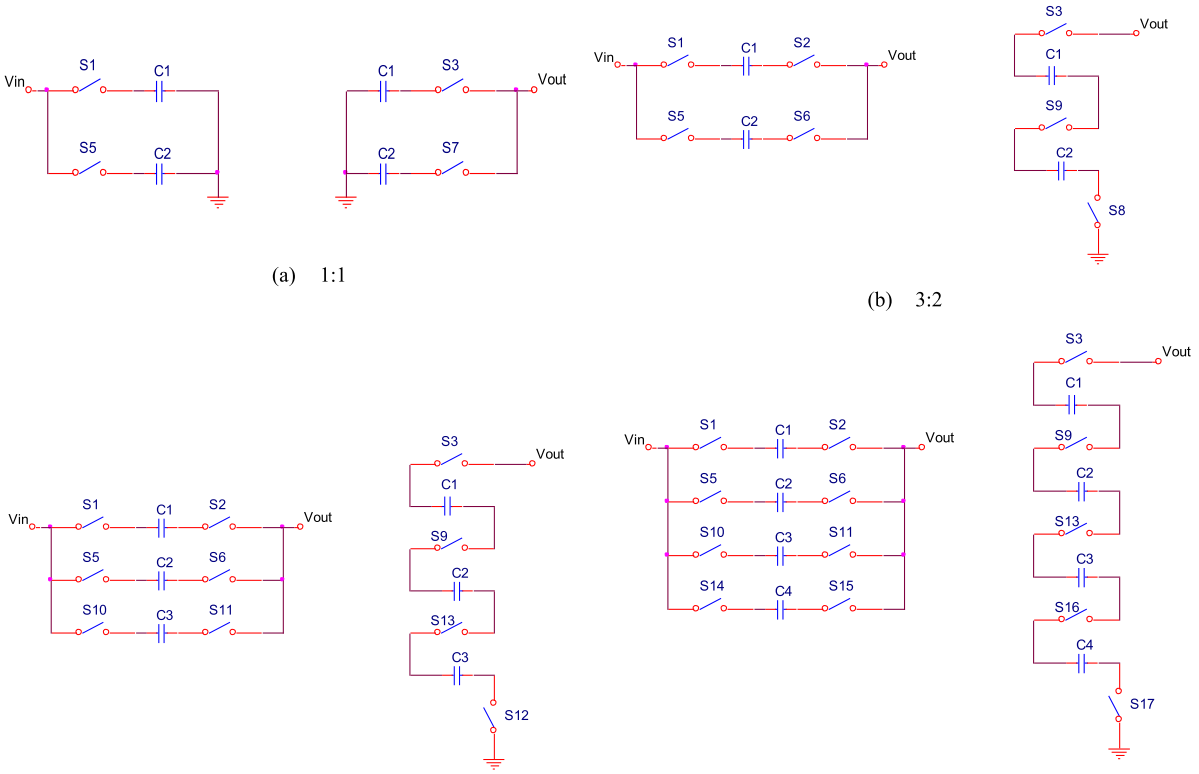


FIGURE 3. Reconfigurable SCVR core.

TABLE 1. Reconfigurable SCVR nominal output voltage for varying supply voltages (1.24V, 1.15V and 1.03V).

Mode	Ideal V_{out}(V) (V_{in}=1.24V)	Ideal V_{out}(V) (V_{in} =1.15V)	Ideal V_{out} (V) (V_{in}=1.03V)
1:1	1.24	1.15	1.03
5:4	0.992	0.92	0.824
4:3	0.93	0.8625	0.7725
3:2	0.826667	0.766666	0.6866667



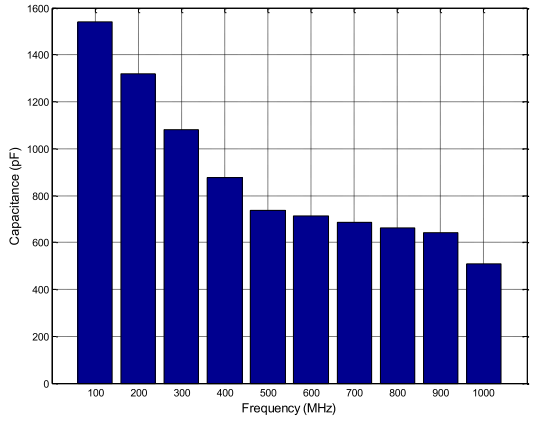
Gain	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	φ_1	off	φ_2	on	φ_1	off	φ_2	on	off
4/5	φ_1	φ_1	φ_2	off	φ_1	φ_1	off	off	φ_2
3/4	φ_1	φ_1	φ_2	off	φ_1	φ_1	off	off	φ_2
2/3	φ_1	φ_1	φ_2	off	φ_1	φ_1	off	φ_2	φ_2
Gain	**S10**	**S11**	**S12**	**S13**	**S14**	**S15**	**S16**	**S17**	
1	off	off	off	off	off	off	off	off	
4/5	φ_1	φ_1	off	φ_2	φ_1	φ_1	φ_2	φ_2	
3/4	φ_1	φ_1	φ_2	φ_2	off	off	off	off	
2/3	φ_2	off	off	off	off	off	off	off	

(e)

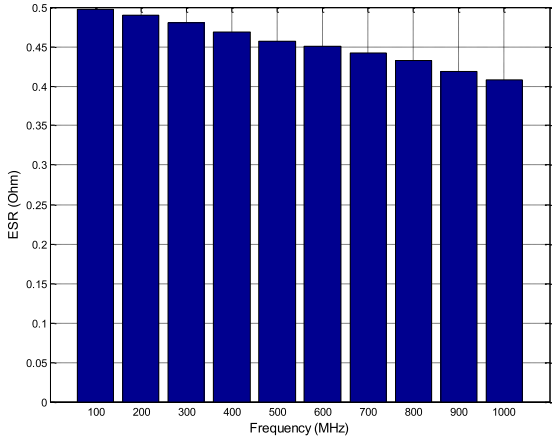
FIGURE 4. SCVR core reconfiguration for various VCRs (a) 1:1 (b) 3:2(c) 4:3 (d) 5:4 (e) Static control signals for different gain configurations of SCVR.

2) TWO-PHASE INTERLEAVING

One typical method used in SCVR design to minimize output ripple is interleaving [21], [25]. Using this technique, the SC regulator is divided into multiple smaller units, each of which receives phase-shifted clock signals about the others. Fig. 6 illustrates a basic two-phase interleaved SCVR. This method has multiple benefits: it reduces ripples in the output voltage and current without requiring extra decoupling capacitors for the input and output stages. The unit cells in different converter blocks are fed with interleaved clock phases to reduce output ripple voltage. However, with a ±5% manufacturing tolerance in capacitors, phase mismatch can occur, leading to uneven charge transfer between the interleaved phases. This can result in increased output ripple due to phase imbalance and uneven phase current distribution. While interleaving helps mitigate some mismatch effects, the capacitor tolerance introduces variations that may slightly degrade voltage stability. However, using tighter tolerance capacitors (±1%) or active balancing techniques helps to maintain optimal performance. To reduce output ripple in a single-phase implementation, large decoupling capacitors are usually needed, which results in a significant increase in on-chip area. When N-phase interleaving is used, flying capacitors in the other N-1 phases effectively reduce the



(a)



(b)

FIGURE 5. Frequency response of MIM capacitor: (a) Capacitance and (b)ESR variation with switching frequency of operation.

TABLE 2. Capacitance modeling parameters.

Element	No. of elements	Values
Number of cells	2	-
MIM capacitors/cell	2(1 for each C_{fly})	0.4nF (for each C_{fly})
Number of MIM capacitor	4	0.4nF (each)
Capacitance/Tile	-	400pF
Number of tiles	4	1.6nF
Equivalent ESR for 1.6nF @ 100MHz	-	0.5Ω

decoupling effect, resulting in a lower output ripple, whenever the flying capacitor changes states between charging and discharging. Further, Fig. 7 displays the top-level architecture of the power management IC (PMIC). To reduce output voltage ripple, this design incorporates a reconfigurable SCVR split into two modules (M1 and M2) that are interleaved [26]. A clock generator, a voltage reference, a gain selection block and pulse frequency modulation (PFM) regulatory circuitry are included in the architecture. Fig. 7 illustrates a clock generator (Cl) that delivers two non-overlapping clock phases; φ_1 and φ_2, to prevent short-circuit current from input to the ground during the switching process.

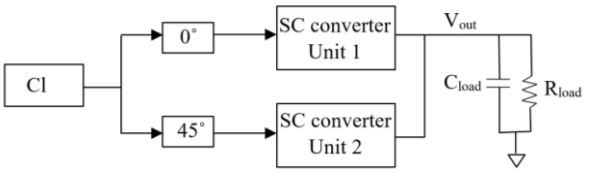


FIGURE 6. A simple two-phase interleaved SC converter.

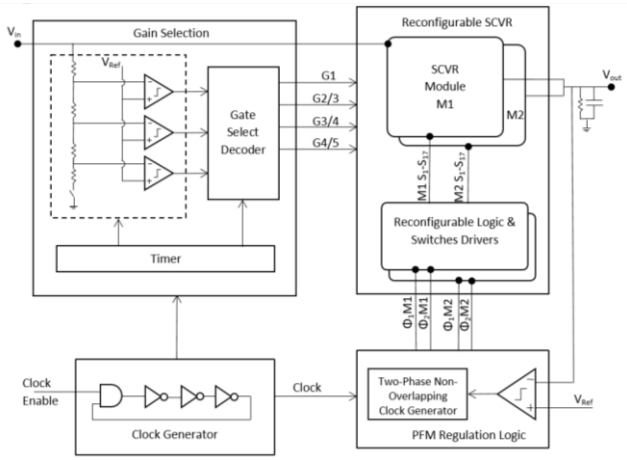


FIGURE 7. Overall architecture of power management IC.

B. SCVR LOSS ANALYSIS

The 3:2 step-down converter, which is presented in Fig. 4 (b), is used to describe the basic working of SC converters. Each switch in the converter has a 50% duty cycle and operates in two phases namely common mode (φ_1) and gain mode (φ_2). The converter may operate in either common mode or gain mode by changing the switch configuration during each phase. There are total of seven switches, two flying capacitors and one load capacitor (single phase). During φ_1, C_1 and C_2 are charged to (V_{in}–V_{out}), whereas in φ_2, C_1 and C_2 are in series connection and the total voltage at the output node is calculated as $V_{out} = 2(V_{in} - V_{out})$, resulting into $V_{out} = 2/3$. As converter operates in two regions of operation namely SSL and FSL modes of operation. The charge multiplier vector for capacitors (a_c) is given as

$$a_c = [1/3\ 1/3\ 1/3\ 1/3] \tag{4}$$

From equation (1), $(a_c)^2$ is calculated as 4/9. Using equation (1), the SSL impedance is calculated as

$$R_{SSL} = \frac{4/9}{C_{fly} f_{sw}} \tag{5}$$

In equation (5) C_{fly} is the total flying capacitance of the unit cell and f_{sw} is the switching frequency of the converter. For the two-phase 3:2 SP converter, the total R_{SSL} will be half of the earlier (which is for a single phase).

For FSL calculation, the switch charge-multiplier vector (a_r) in φ_1 is specified as

$$a_r = [1/3\ 1/3\ 1/3\ 1/3] \tag{6}$$

In the case of φ_2, the charge-multiplier vector is given as

$$a_r = [1/3\ 1/3\ 1/3] \tag{7}$$

For calculation of FSL output impedance, the charge multiplier vector for switches in both phases is given as:

$$a_r = [1/3\ 1/3\ 1/3\ 1/3\ 1/3\ 1/3] \tag{8}$$

The value for the above metric is computed as $(a_r)^2 = 7/9$. Substituting this value in equation (2) results in FSL impedance (R_{FSL}) as

$$R_{FSL} = {}^{14}\!/_{9}\, R_{on} \tag{9}$$

For two-phase converter:

$$R_{FSL} = {}^{7}\!/_{9}\, R_{on} \tag{10}$$

In equation (10), R_{on} is switched on-resistance and R_{FSL} is the FSL output impedance and is independent of frequency. The power loss due to SSL, FSL and ESR impedances is given as

$$P_{SSL} = R_{SSL} I_{out}^2 \tag{11}$$
$$P_{FSL} = R_{FSL} I_{out}^2 \tag{12}$$
$$P_{esr} = R_{esr} I_{out}^2 \tag{13}$$

The converter's equivalent output impedance is calculated as

$$R_{\text{eq}} \approx \sqrt{R_{SSL}^2 + (R_{FSL} + R_{esr})^2} \tag{14}$$

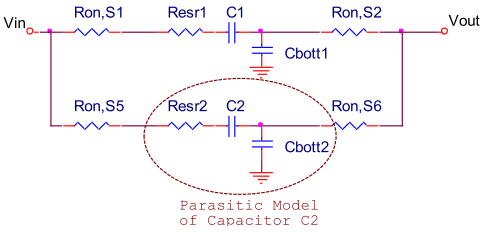
The conduction power loss (P_{cond}) is directly proportional to the impedance (R_{eq}) given as

$$P_{cond} = R_{\text{eq}} I_{out}^2 \tag{15}$$

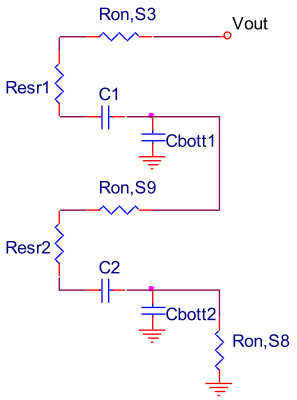
There exist several categories of losses, defined as follows:

- Gate drive loss is the result of operating the charge transfer switches gates. This loss is a function of the applied voltage, the switching frequency, and the total switch area.
- The capacitor's bottom plate loss occurs due to charging loss of the parasitic capacitance on the bottom plate. It is dependent on the switching frequency and the parasitic capacitance.

These losses are investigated in the proposed SCVR in order to achieve optimal design parameters and enhanced power efficiency as shown in Fig. 8. Table 3 shows the detailed power loss breakdown of the reconfigurable SCVR. The primary source of loss is parasitic capacitors, which are



(a) Phase-1



(b) Phase-2

FIGURE 8. Two-phase 3:2 series-parallel SCVR parasitic model including C_{bott}, C_{sw} and ESR.

inherent to the on-chip capacitor fabrication process and usually restrict the converter's optimal performance. These losses arise when flying capacitors are charged and discharged to power the load. The charging and discharging of the bottom plate capacitor, $C_{bott} = \alpha C_{fly}$, for every clock cycle is an undesirable outcome of this process where α is technology dependent parameter. Incorporating MIM capacitors for charge transfer that have low bottom plate parasitic provides efficient power conversion. Since the flying capacitor capacitance and the load current are closely correlated, high-density on-die MIM capacitors enable the load's power requirements to be satisfied without requiring a significant area overhead. The power loss due to the flying capacitor's bottom plate (P_{bott}) and switch-related (P_{sw}) parasitics are expressed as

$$P_{bott} = N_C C_{bott} V_c^2 f_{sw} \tag{16}$$
$$P_{sw} = N_s C_{sw} V_{sw}^2 f_{sw} \tag{17}$$

In equation (16), C_{bott} is the bottom-plate parasitic capacitance. N_C represents the number of capacitor (or the total MIM cap area) and the bottom-plate capacitor voltage is denoted by V_C. Additionally, switch parasitic capacitance, number of switches (switch size), switching frequency, and switch blocking voltage are represented by C_{sw}, N_s, f_{sw}, and V_{sw}, respectively, in equation (17). Hence, the total power loss is given by

$$P_{loss} = P_{cond} + P_{bott} + P_{sw} \tag{18}$$

TABLE 3. Power loss breakdown of reconfigurable SC DC-DC converter.

VCR	Average V_{out} (V)	Average I_{out} (mA)	P_{in} (W)	P_{out} (W)	SSL loss(W)	FSL loss(W)	C_{bott} loss(W)	C_{sw_cap} loss(W)	ESR loss(W)	Total Loss(W)
5:4	0.85666	387.627	0.41326	0.33206	0.04791	0.03004	0.00162	0.00081	0.00244	0.08120
4:3	0.76013	304.052	0.29548	0.23112	0.03990	0.01673	0.00064	0.00032	0.00708	0.06436
3:2	0.65992	203.051	0.17482	0.13410	0.02817	0.00734	0.00082	0.00041	0.00460	0.04082
1:1	0.98388	614.925	0.78452	0.60501	0.09694	0.06103	0.00180	0.00091	0.01795	0.17951

The actual output voltage and power are expressed as

$$V_{out,actual} = V_{out} - R_{eq} I_{out} \tag{19}$$

$$P_{out,actual} = V_{out,actual} I_{out} \tag{20}$$

In equation (19), V_{out} is the nominal output voltage. Using equations (18), (19), and (20), the efficiency (η) of the two-phase 3:2 SCVR operating in SP configuration is given by

$$\eta = \frac{P_{out,actual}}{\left(P_{out,actual} + P_{loss}\right)} \tag{21}$$

It is necessary to minimize losses to calculate the optimal efficiency for an area-limited SCVR design.

$$\eta_{opt} = \frac{P_{out,actual}}{P_{out,actual} + P_{loss,min}} \tag{22}$$

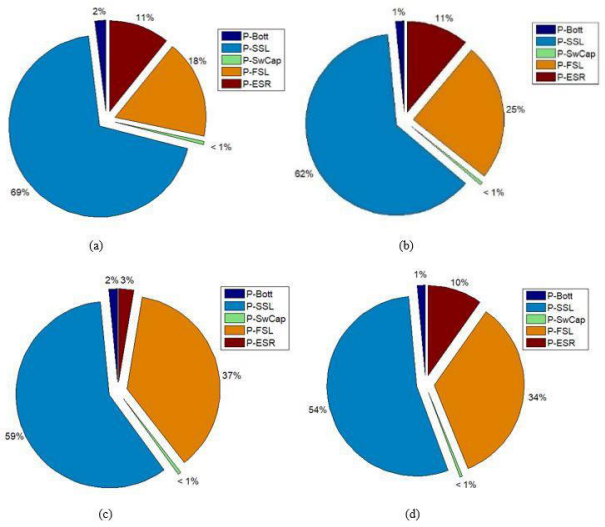


FIGURE 9. Power loss distribution chart for the reconfigurable MIM capacitor SC converter (a) 3:2 (b) 4:3 (c) 5:4 (d) 1:1

The conduction, switching and parasitic loss is the conversion power loss ($P_{loss,min}$) given by equation (22). The two-phase 3:2 SCVR achieves optimal efficiency by employing an interior-point approach to determine the minimal power loss for varying load currents and flying capacitance values. A similar analysis is done for converter topologies with conversion ratios of 5:4, 4:3 and 1:1.

Fig. 9 provides a comprehensive power loss breakdown of the reconfigurable SC DC-DC converter in detail, showing how these losses affect converter efficiency and overall system performance. As switching frequency increases, this energy loss scales linearly with frequency, but the total gate capacitance also grows with increasing parallel switches (used to reduce conduction loss), leading to a non-linear increase in P_{sw}. To mitigate switching losses especially at high frequencies, several architectural and circuit-level techniques are used. Some of them are switch sizing based on trade-off between conduction loss and dynamic loss and use of multiple interleaved phases where each switch toggles at lower effective frequency reducing the total dynamic loss. Power device optimization is critical for high efficiency concern. The power losses in the proposed unit cell includes the charge redistribution loss of flying capacitors, the conduction loss of switch on-resistance, the gate charging loss and the bottom plate parasitics loss. The two dominant losses are capacitive and resistive loss. This is because when the capacitance density increases, the total capacitance for the same area will increase. Further, with lower operating frequencies switches can be of much larger size to reduce FSL's resistive loss. Hence, converter's overall performance is enhanced by minimizing these losses, mostly by the use of low-ESR capacitors utilizing MIM tile structures and switch size optimization techniques. However, the losses from gate drives and bottom-plate capacitors are not significant in this design, but they become more evident in other topologies or at higher switching frequencies. This table demonstrates the trade-off between VCR and power loss. Further, with higher step-down ratios exhibiting greater charge redistribution losses. The added comparison helps clarify performance trends across all supported configurations.

IV. EFFICIENCY OPTIMIZATION

For a given output impedance, this section explains optimization approaches that enable effective utilization of capacitor energy storage and switch silicon area [19]. Regulation is divided into two distinct phases. Selecting the conversion topology for course adjustments is the first phase. The SCVR's output resistance is adjusted in the second phase. A feedforward control circuit simplifies the topology selection by utilizing data on input and output voltage levels. As covered in Section III, the SCVR has several design characteristics, such as C_{fly}, f_{sw}, and N_s (switch size), that affect power losses. All of these variables have a different impact on the SCVR's overall performance. Additionally, operating parameters like V_{out} and I_{out} have also influenced

power efficiency. Improved power efficiency for the SCVR can be achieved by minimizing power losses depending on operating conditions and design parameters [27].

A. SWITCH SIZE OPTIMIZATION

The losses incurred in recharging MOS switch gate capacitance must be considered in a fully integrated SCVR design because these devices operate at frequencies far higher than those of inductive converters with discrete external capacitors. Optimizing SC DC-DC converters to achieve optimal efficiency within the desired range of operating voltages requires careful evaluation of all major sources of loss. To enhance conductivity, it is preferable to place multiple switches in parallel. The converter design employing MIM capacitors may significantly enhance light load efficiency by varying the MOSFET width [17], [18], [19]. Fig. 10 illustrates how efficiency changes as switch size (N_s) increases. The value of switch conductance increases as N_s increases because the equivalent switch resistance R_{on}/N_s decreases.

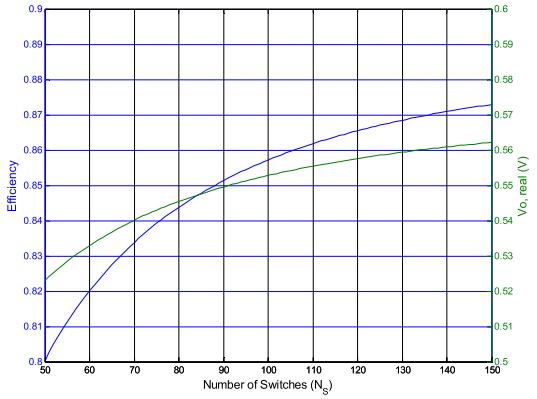


FIGURE 10. Efficiency and $V_{out,actual}$ variation with N_S(switch width) for f_{sw} = 100 MHz and ESR = 0.5Ω.

B. OPTIMUM SWITCHING FREQUENCY

The device parasitic (described in section III-A) determines the maximum feasible fsw based on the process technology utilized to implement SCVR [20], [21]. The converter is required to operate at this switching frequency while it is at maximum load. The efficiency variation with changing f_{sw} is shown in Fig. 11. Further, with an increase in f_{sw} the parasitic loss also increases which results in decreased efficiency. A summary of the different circuit and control parameters used in the simulation is given in Table 4.

C. CAPACITOR SELECTION: OUTPUT RIPPLE VOLTAGE

The ripple voltage and current determine the output capacitor selection initially. The output ripple voltage is largely influenced by the capacitor's equivalent series resistance (ESR). By utilizing the ripple current (ΔI_L) and the ESR of the capacitor, the output ripple voltage can be easily approximated by using the capacitor's ESR and ΔI_L. Therefore, a capacitor with the lowest possible ESR is preferable.

TABLE 4. Optimized design parameters.

Parameter	Value Assigned
V_{in}	1.24 V
R_{load}	3 Ω
Switch size(each cell)	0.48µ /0.03µ, PMOS/NMOS
N_s	100
Equivalent R_{on}	0.8Ω (80Ω /100)
f_{sw} (Sweep)	50 MHz to 1 GHz

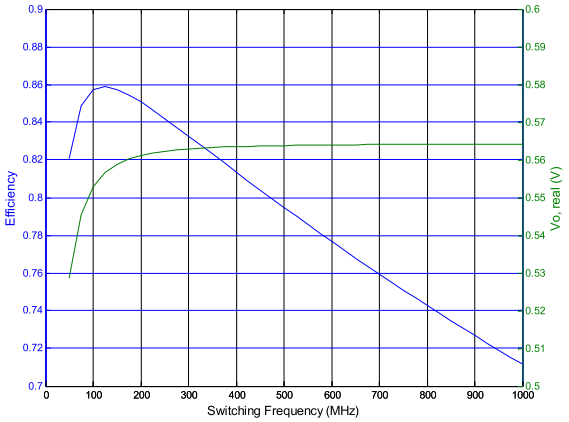


FIGURE 11. Efficiency and $V_{out,actual}$ tradeoffs with f_{sw} for R_{on} = 0.8Ω (N_S = 100)and ESR=0.5Ω.

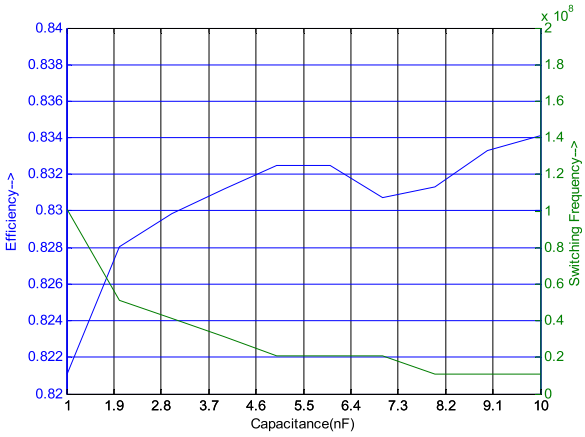


FIGURE 12. Efficiency and f_{sw} variation with capacitance.

MIM capacitor tile structure helps in reducing bottom-plate capacitance and ESR. A tile structure means the large capacitor area is divided into smaller, repeated capacitor "tiles" arranged in parallel. Each tile has a smaller bottom plate area. Since parasitic bottom-plate capacitance is proportional to the overlapping area between the bottom plate and the substrate or other layers, dividing the capacitor into smaller tiles reduces the effective parasitic overlap per tile. Each tile acts as a small capacitor cell. The MIM Tile performance parameters are shown in Table 5 [22]. To validate the accuracy of the proposed optimization methodology and

TABLE 5. MIM Tile performance parameters.

Parameters	Corehby2 structure	Coreh structure	Units
MIM density	15	15	fF/μm^2
MIM Utilization	85	85	%
Effective MIM density	13.3	13.3	fF/μm^2
MIM Cap area for 1nF	0.0752	0.07516	mm^2
Load current density	400	400	mA/mm^2
Effective load current per 1nF of cap	30.0625	30.0625	mA
Effective load current per 1.6nF of cap	48.1	48.1	mA
ESR for 1.6nF MIM Cap	0.50	0.57	Ω
Equivalent cap obtainable in 1mm^2	13.3056	13.3056	nF
No. of tiles supported per core	4	2	-
Total cap supported	1.6	1	nF
Total load current supported	48.1	48.1	mA
MIM Cap area for 1 tile (400/800pf)	0.0300625	0.060125	mm^2

TABLE 6. Design parameters.

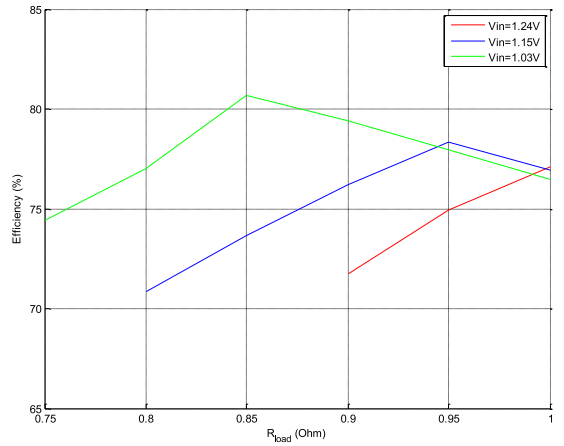
Input Parameter	Value
V_{in}	1.24V, 1.15V, 1.03V
VCRs	5:4, 4:3, 3:2, 1:1
R_{load}	1Ω-3.25 Ω
R_{on} of the unit switch cell	80 Ω
C_{sw}	15 fF
C_{fly}	0.4 nF
C_{bott}	C_{fly}/constant
ESR (for C_{fly})	0.5 Ω

TABLE 7. Reconfigurable SCVR target load current and output voltage profiles.

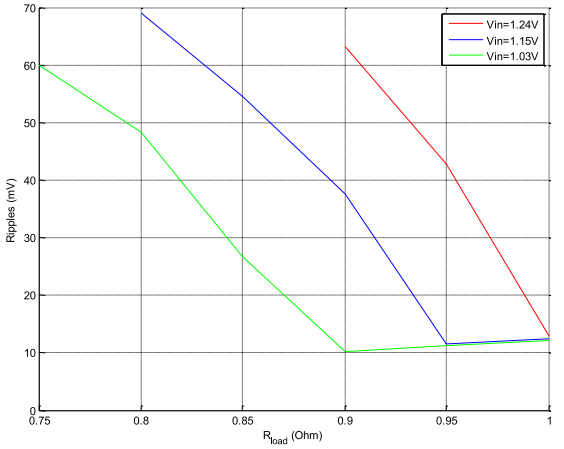
Target V_{out}(V)	Mode V_{in}=1.24V	Mode V_{in} =1.15V	Mode V_{in} =1.03V	I_{load} (mA)
1	1:1	1:1	1:1	625
0.95	1:1	1:1	1:1	535.86
0.9	1:1/5:4	1:1	1:1	455.63
0.85	5:4	1:1/5:4	1:1	383.83
0.8	5:4	1:1/5:4	1:1	350
0.75	4:3	5:4	1:1/5:4	300
0.7	3:2	4:3	5:4	250
0.65	3:2	3:2	4:3	200
0.6	3:2	3:2	3:2/4:3	200

our analytic model of the output impedance, the simulation of each topology is performed with a parasitic capacitance added to each MIM capacitor of the capacitor array topology. The different optimized topologies are implemented and simulated on circuit level to validate the results. For light loads or applications where ripple is less significant, smaller capacitors can be used. The current needed by the load must be supplied by the output capacitor in the interval between the load transient and the P-MOSFET turning on. The voltage drop across the ESR is caused by the current delivered by the output capacitor. A capacitor with low ESR reduces the voltage loss when delivering load current. The parasitic ESR of 0.5 Ω per 1.6nF at 100MHz reflects a combined contribution from parasitic interconnect resistance, bottom-plate losses, and switch resistance, rather than the intrinsic ESR of the MIM capacitor alone. MIM capacitors, especially those fabricated in deep sub-micron processes with stacked metal layers, typically exhibit very low intrinsic ESR (in the range of milliohms). However, when placed within a high-frequency SC converter, additional loss mechanisms such as bottom-plate charge loss and resistive routing can collectively appear as an effective ESR in the system-level model. The ESR value of 0.5 Ω is a system-level effective ESR, extracted under dynamic switching conditions. To address this, tiled MIM capacitor structures [22] are implemented for uniform current distribution. Further, interleaved and reconfigurable conversion modes are utilized to distribute current load and reduce per-path loss. These measures limits the ESR-induced efficiency degradation, particularly at high switching frequencies. Switch conductance modulation is one of the techniques that is considered for enhancing efficiency and minimizing voltage ripple for light loads [16], [20]. Additionally, interleaved designs also aid in reducing voltage ripple. On the other hand, the ripple may grow rather large for heavy loads [13].

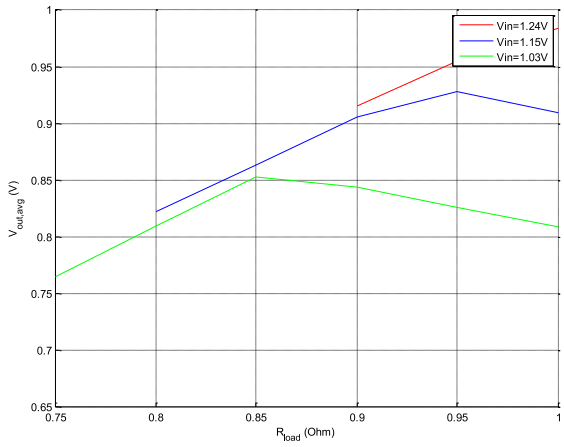
In a given topology, each C_{fly} is proportional to the appropriate charge multiplier coefficient ($a_{c,i}$). In a step-down SC topology, the number of C_{fly} cells (N_c) needed varies with the topology reconfiguration as stated in [5]. This equivalent-output-impedance model suggests that the PCE design consideration can be transformed into a design process that aims to achieve the best capacitance sizing ratio, and consequently, the lowest R_{SSL}.



(a)

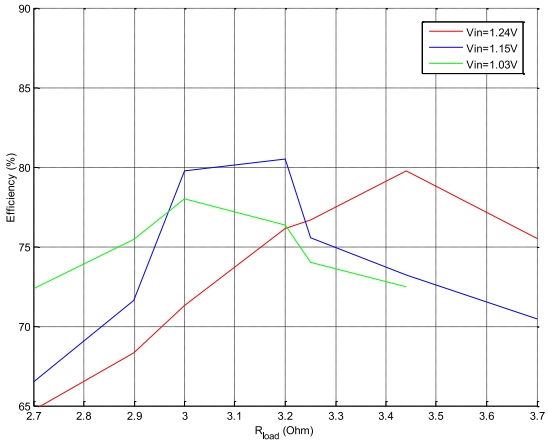


(b)

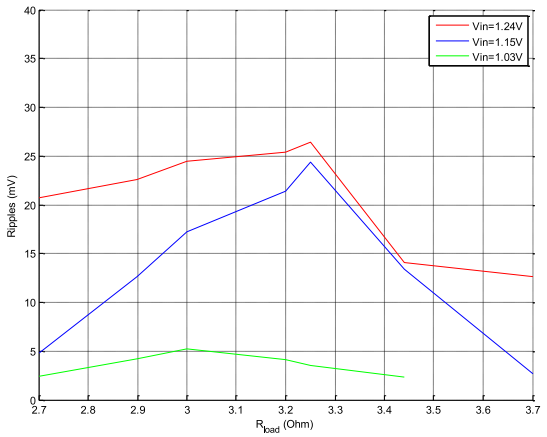


(c)

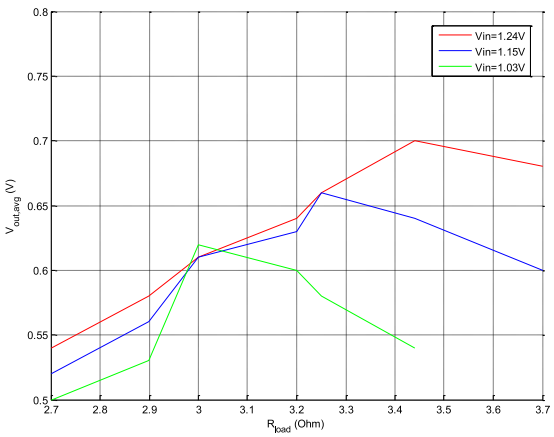
FIGURE 13. SC converter simulated (a) efficiency, (b) ripple and (c) output voltage variation, with load resistance for 1:1 gain configuration.



(a)



(b)



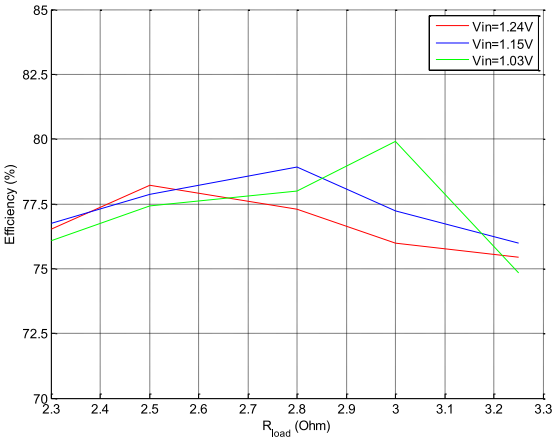
(c)

FIGURE 14. Simulated SC converter (a) efficiency, (b) ripple and (c) output voltage variation, with load resistance for 3:2 gain configuration.

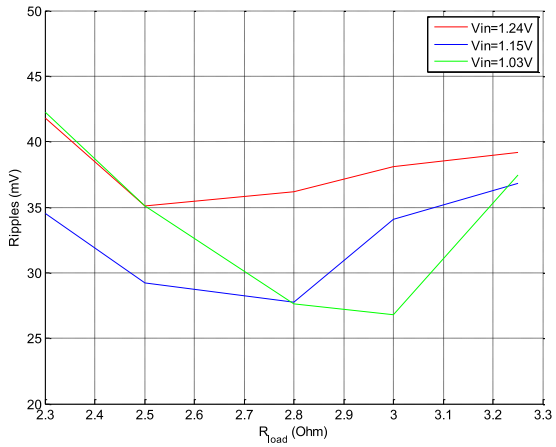
The efficiency and f_{sw} variation with capacitance for an I_{load} value of 48mA and a current density of 400mA/mm^2 are shown in Fig. 12. The R_{SSL} impedance decreases as capacitance increases. Further, f_{sw} drops as C_{fly} increases, which lowers parasite loss and maximizes efficiency.

V. SIMULATION RESULTS

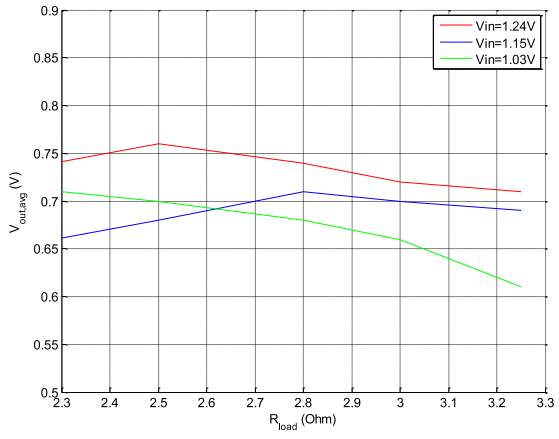
This section describes the efficiency results for two-phase interleaved reconfigurable SCVR for different I_{load} and target V_{out} having VCRs as 1:1, 3:2, 4:3 and 5:4. (Schematic



(a)

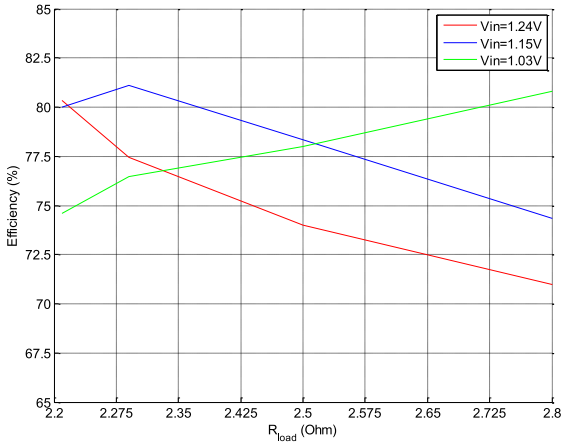


(b)

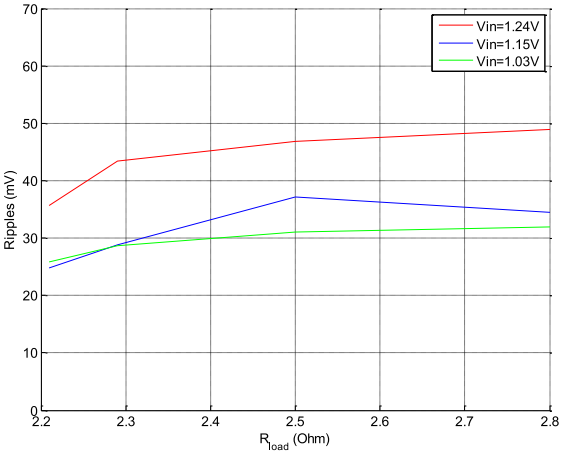


(c)

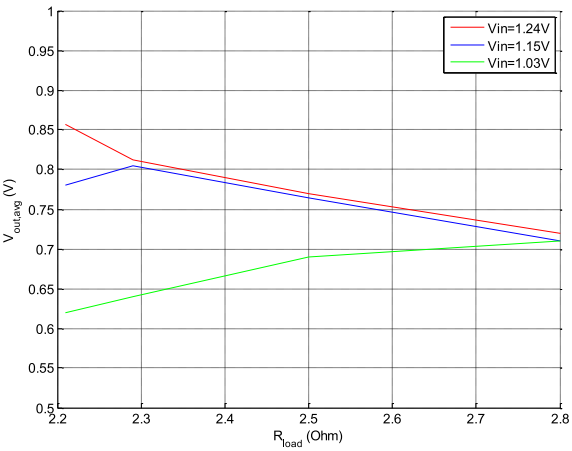
FIGURE 15. Simulated SC converter (a) efficiency,(b) ripple and (c) output voltage variation, with load resistance for 4:3 gain configuration.



(a)



(b)



(c)

FIGURE 16. SC converter simulated (a) efficiency, (b) ripple and (c) output voltage variation, with load resistance for 5:4 gain configuration.

shown in Figs. 3 and 4). The network consists of seventeen switches and four flying capacitors, C_1-C_4, their charging and discharging are accordance to switching clock phases, responsible for reconfiguring the network into four different topologies. The proposed SCVR is designed for target I_{load} of 200mA to 625mA with a high-density MIM capacitor

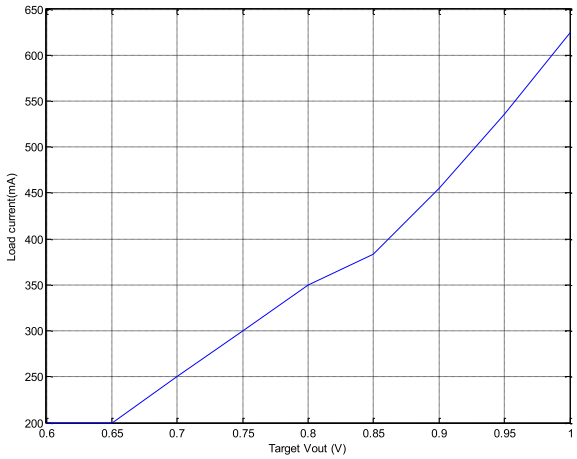


FIGURE 17. Reconfigurable SCVR target load current profile with output voltage.

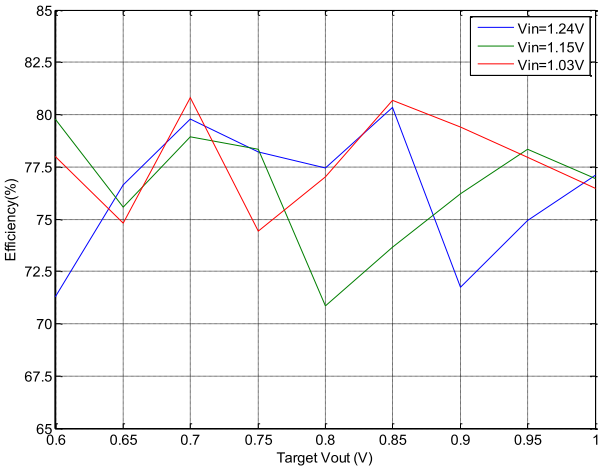


FIGURE 19. Reconfigurable SCVR efficiency variation with output voltage.

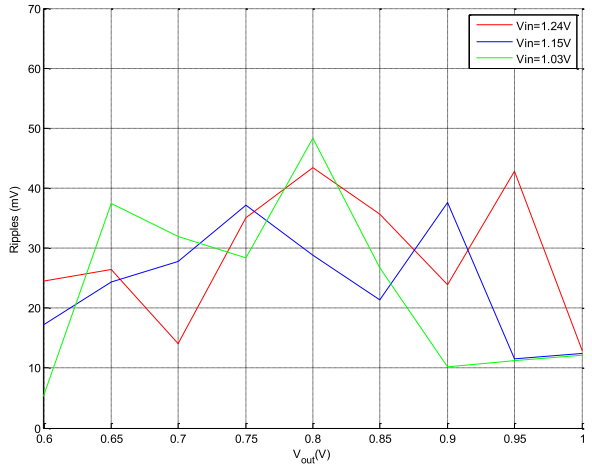


FIGURE 18. Reconfigurable SCVR ripple variation with output voltage.

implemented in 22nm tri-gate CMOS for target V_{out} ranging from 0.6V to 1V. The values of V_{GS} and R_{on} are 0.9V and 0.8Ω (for $N_s = 100$) respectively, which is equivalent to the switch size of $0.48\mu/0.03\mu$ (PMOS/NMOS) @110°C evaluated by considering multiple numbers of this basic switch. Further, the total gate capacitance C_{sw} (C_{gs}+C_{gd} +C_{db}) of the unit switch cell is $C_{sw} = 15$fF and C_{fly} value is taken as 0.4nF. The various MIM capacitor design parameters are presented in Table 5. The C_{bott} is defined as $C_{bott} = C_{fly}$/constant and for constant value 1000, C_{bott} becomes 4pF. In simulation, ideal components are assumed and parasitic elements are explicitly included as additional capacitors or resistors as shown in Fig. 8. For two-phase interleaved reconfigurable SCVR, the average V_{out}, efficiency and ripple at the outputs for three input voltages (V_{in}) 1.24V, 1.15V and 1.03V are computed for each conversion ratio. Various cross-corner analyses have been done for each topology as shown in Figs. 13-16. The design parameters used in PSpice simulation are presented in Table 6. Further, Figs. 17-19 shows efficiency, ripple and target load current variations with target output voltage for two-phase interleaved reconfigurable SCVR operating in different modes to attain the desired target V_{out} and load current as shown in Table 7.

At an input voltage of 1.03 V, the converter operates close to a unity conversion ratio (e.g. 5:4 or 4:3), depending on the mode. In this case, the voltage difference across flying capacitors is relatively small, so the amount of charge redistributed per cycle is reduced helps in reducing the output ripple. Therefore, based on this balance of reduced swing and enhanced susceptibility to parasites, ripple voltage remain somewhere in the intermediate range. Interleaving means the use of multiple converter phases operating in parallel but switching at time or phase shifted intervals.

Further, splitting the load current between two phases means each handles roughly 100mA to 312.5mA for the target load current of 200mA to 625mA. Hence, the ripple current per phase decreases. By distributing the load current and doubling the switching frequency via interleaving, the output ripple can be reduced below 50mV at low R_{load} (< 2.5 Ω). The converter can be reconfigure to a different VCR to reduce output ripple, even if the target output voltage is the same. This is especially useful when operating at low V_{in} or high load currents. In addition, ripple analysis of various conversion ratios of SCVR are shown in Tables 8-11.

Table 12 presents a comparison between the proposed work and the existing SC converters. Performance metrics used in the comparison, include capacitor technology, peak efficiency, load current density, output voltage, switching frequency, ESR and unit cell MIM capacitance. This work utilizes an on-die MIM capacitor of 1.6nF capacitance due to high capacitance utilization per unit area with the lowest parasitic (ESR and C_{bott}), as shown in Fig. 5 (a) and (b).

TABLE 8. Output ripple analysis of 5:4 SCVR mode.

C_{load} (nF)	V_{ref_scvr} (V)	R_{load} (ohms)	V_{cc} (V)	skew	temp	V_{out_ideal} (V)	V_{out_avg} (V)	Efficiency (%)	Ripple (V)
6	0.9	1.98	1.24	tttt	70	0.992	0.89	84.57	0.0239
6	0.85	2.21	1.24	tttt	70	0.992	0.86	80.35	0.0356
6	0.8	2.29	1.24	tttt	70	0.992	0.81	77.45	0.0434
6	0.85	2.21	1.15	tttt	70	0.92	0.84	82.14	0.0214
6	0.8	2.29	1.15	tttt	70	0.92	0.80	80.09	0.0288
6	0.75	2.5	1.15	tttt	70	0.92	0.76	78.35	0.0372
6	0.75	2.5	1.03	tttt	70	0.824	0.75	81.12	0.0284
6	0.7	2.8	1.03	tttt	70	0.824	0.71	80.81	0.0320

TABLE 9. Output ripple analysis of 4:3 SCVR mode.

C_{load} (nF)	V_{ref_scvr} (V)	R_{load} (ohms)	V_{cc} (V)	skew	temp	V_{out_ideal} (V)	V_{out_avg} (V)	Efficiency (%)	Ripple (V)
6	0.75	2.5	1.24	tttt	70	0.93	0.76	78.22	0.0351
6	0.7	2.8	1.15	tttt	70	0.8625	0.71	78.93	0.0278
6	0.6	3	1.03	tttt	70	0.7725	0.66	79.92	0.0268
6	0.65	3.25	1.03	tttt	70	0.7725	0.61	74.82	0.0374

TABLE 10. Output ripple analysis of 3:2 SCVR mode.

C_{load} (nF)	V_{ref_scvr} (V)	R_{load} (ohms)	V_{cc} (V)	skew	temp	V_{out_ideal} (V)	V_{out_avg} (V)	Efficiency (%)	Ripple (V)
6	0.6	3	1.24	tttt	70	0.83	0.61	71.28	0.0245
6	0.65	3.25	1.24	tttt	70	0.83	0.66	76.65	0.0264
6	0.7	3.44	1.24	tttt	70	0.83	0.7	79.77	0.0141
6	0.6	3	1.15	tttt	70	0.77	0.61	79.78	0.0172
6	0.65	3.25	1.15	tttt	70	0.77	0.66	75.56	0.0244
6	0.6	3	1.03	tttt	70	0.69	0.6	77.99	0.0053

TABLE 11. Output ripple analysis of 1:1 SCVR mode.

C_{load} (nF)	V_{ref_scvr} (V)	R_{load} (Ω)	V_{cc} (V)	skew	temp	V_{out_ideal} (V)	V_{out_avg} (V)	Efficiency (%)	Ripple (V)
6	1	1.6	1.24	tttt	70	1.24	0.98	77.12	0.0129
6	0.95	1.77	1.24	tttt	70	1.24	0.95	74.94	0.0428
6	0.9	1.98	1.24	tttt	70	1.24	0.92	71.75	0.0632
6	1	1.6	1.15	tttt	70	1.15	0.91	76.94	0.0125
6	0.95	1.77	1.15	tttt	70	1.15	0.93	78.35	0.0115
6	0.9	1.98	1.15	tttt	70	1.15	0.91	76.20	0.0376
6	0.85	2.21	1.15	tttt	70	1.15	0.86	73.65	0.0546
6	0.8	2.29	1.15	tttt	70	1.15	0.82	70.84	0.0690
6	1	1.6	1.03	tttt	70	1.03	0.81	76.46	0.0121
6	0.95	1.77	1.03	tttt	70	1.03	0.83	77.94	0.0112
6	0.9	1.98	1.03	tttt	70	1.03	0.84	79.42	0.0102
6	0.85	2.21	1.03	tttt	70	1.03	0.85	80.69	0.0268
6	0.8	2.29	1.03	tttt	70	1.03	0.81	77.03	0.0484
6	0.75	2.5	1.03	tttt	70	1.03	0.77	74.44	0.0599

The use of frequency scaling technique and switch width modulation (N_s) in deriving minimum power loss aided in achieving the peak efficiency of 81.09 % for the proposed two-phase interleaved reconfigurable SCVR operating at

TABLE 12. State-of-art comparison.

Design	[7]	[11]	[15]	[16]	[19]	[20]	[21]	[13]	This work
Result	Sim.	Sim.	Sim.	Mea.	Sim.	Mea.	Sim.	Mea.	Sim.
Process	65 nm	180 nm	0.25 µm	180 nm	-	0.18 µm	0.18 µm	0.18 µm	22 nm
VCR	5:2, 3:1	2:1	2:1	2:1, 3:1, 3:2	16:1	3:2, 5:3, 2:1, 5:2	2:1	3:1, 2:1	5:4, 4:3, 3:2, 1:1
Capacitor	MOS	MOS	MIM	Off-chip	Gate oxide	MIM	MIM	MOS	MIM
C_{fly}	3.88nF	6nF	200 pF	1µF	33µF	500 pF	515pF	100pF	1.6nF
V_{in}	3-4V	1.8V	0.6-2.4V	2.5 to 4.5V	48V	2.7V	2V	1.8V	1.03V, 1.15V, 1.24V
V_{out}	1V	0.85V	1.2V	1V	3V	1.2V	0.9V	0.5-0.85V	0.6-1V
I_{load}	-	1.5mA	100µA	1-10 mA	1A	2mA	12µA-17.8mA	1.4-5mA	**200-625 mA**
f_{sw}	-	10 MHz	-	100 KHz	500 KHz	2-20 MHz	20KHz-49MHz	-	**100MHz**
η	73%	80%	76%	70.8%	83%	84.2%	80%	74%	**81.6%**

an optimum switching frequency of 100MHz as shown in Fig. 19.

VI. CONCLUSION

Per-core regulation for microprocessor power supply with granular power delivery could greatly increase future data centers energy efficiency. On-chip SCVR with its high efficiency and high power density architecture can allow for such granular power delivery with per-core regulation. This paper details the implementation of fully integrated two-phase interleaved reconfigurable SCVR in a 22 nm CMOS technology with high-density MIM capacitors. The proposed converter working principle and its analysis are explained for different operating modes. It supports maximum load current ranges from 200mA to 625mA and achieves 71-81% efficiency. A broad output voltage range of 0.6-1V is provided by the all-digital, multi-conversion-mode SCVR from three distinct source voltages of 1.24V, 1.15V and 1.03V. Reconfigurable SCVRs with multi-gain settings are proposed to enable efficient performance throughout a broad output voltage range. The optimal operating point of the SC converter is also discussed. This work achieves 81.6% peak efficiency and an output power density of 226 mW/mm^2. The proposed converter description, steady-state analysis, and merits related to other converters have been extensively discussed. In addition, we also addressed challenges with SC converters, including their restricted number of conversion ratios and output ripple characteristics for a broad range of output voltage.

DECLARATION

Data Availability Statement: The data will be made available on request.

Conflicts of Interest: There are no potential conflicts of interest.

REFERENCES

[1] H. Bi, Z. Mu, and Y. Chen, "Common grounded wide voltage-gain range DC–DC converter with zero input current ripple and reduced voltage stresses for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, vol. 70, no. 3, pp. 2607–2616, Mar. 2023.

[2] T. Sutikno, A. S. Samosir, R. A. Aprilianto, H. S. Purnama, W. Arsadiando, and S. Padmanaban, "Advanced DC–DC converter topologies for solar energy harvesting applications: A review," *Clean Energy*, vol. 7, no. 3, pp. 555–570, Jun. 2023.

[3] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brändli, and P. A. Francese, "A 10 w on-chip switched capacitor voltage regulator with feedforward regulation capability for granular microprocessor power delivery," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 378–393, Jan. 2017.

[4] S. Saini and D. S. Saini, "Modeling and analysis of step-down switched capacitor DC–DC converter for SoC," in *Proc. 9th Int. Conf. Signal Process. Commun. (ICSC)*, Dec. 2023, pp. 738–742.

[5] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[6] S. Saini, D. S. Saini, and V. Balyan, "Design considerations for power-efficient fully integrated 3:1 switched capacitor DC–DC converter for PV modules," *Electronics*, vol. 13, no. 21, p. 4156, Oct. 2024.

[7] H.-P. Le, J. Crossley, S. R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm^2 at 73% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 372–373.

[8] N. H. Baharudin, T. M. N. T. Mansur, F. A. Hamid, R. Ali, and M. I. Misrun, "Topologies of DC–DC converter in solar PV applications," *Indonesian J. Electr. Eng. Comput. Sci.*, vol. 8, no. 2, pp. 368–374, Nov. 2017.

[9] S. A. Mohammed, H. Dogan, and M. T. Ozgun, "An 85%-efficiency reconfigurable multiphase switched capacitor DC–DC converter utilizing frequency, switch size, and interleaving scaling techniques," *Microelectron. J.*, vol. 67, pp. 155–161, Sep. 2017.

[10] S. Saini and D. S. Saini, "Performance modeling and design techniques for efficiency improvement in on-chip switched-capacitor DC–DC converter," *Wireless Pers. Commun.*, vol. 127, pp. 3379–3405, Jan. 2022.

[11] M. Hokmabadi and M. Taherzadeh-Sani, "An 80%-efficiency switched-capacitor step-down DC–DC converter with switch-width and digital capacitance modulation," in *Proc. 24th Iranian Conf. Electr. Eng. (ICEE)*, May 2016, pp. 335–339.

[12] R. Jain, B. M. Geuskens, S. T. Kim, M. M. Khellah, J. Kulkarni, J. W. Tschanz, and V. De, "A 0.45–1 v fully-integrated distributed switched capacitor DC–DC converter with high density MIM capacitor in 22 nm tri-gate CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 917–927, Apr. 2014.

[13] P.-H. Chen, H.-C. Cheng, and P.-H. Chen, "A fully integrated step-down switched-capacitor DC–DC converter with dual output regulation mechanisms," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 9, pp. 1649–1653, Sep. 2020.

[14] G. Marin, K. Cherniak, V. Subotskaya, E. Bodano, C. Sandner, and A. Bevilacqua, "A reconfigurable switched capacitor DC–DC converter with 1.9–6.3-V input voltage range and 85% peak efficiency in 28-nm CMOS," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 106–109, 2020.

[15] M. Saadat and B. Murmann, "A 0.6 V–2.4 v input, fully integrated reconfigurable switched-capacitor DC–DC converter for energy harvesting sensor tags," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2015, pp. 1–4.
[16] H. F. Nurhuda and Y. Yang, "A three topology-based, wide input range SC DC–DC converter with low ripple and enhanced load line regulation," in *Proc. IEEE 14th Int. Symp. Integr. circuits (ISIC)*, Sep. 2014, pp. 16–18.
[17] T. Souvignet, B. Allard, and S. Trochut, "A fully integrated switched-capacitor regulator with frequency modulation control in 28-nm FDSOI," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4984–4994, Jul. 2016.
[18] Y. Lu, J. Jiang, W.-H. Ki, C. P. Yue, S.-W. Sin, U. Seng-Pan, and R. P. Martins, "20.4 a 123-phase DC–DC converter-ring with fast-DVS for microprocessors," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[19] K. Eguchi, A. Shibata, and Y. Harada, "A direct high step-down DC/DC converter using cascade ring-type converters," *Energy Rep.*, vol. 6, pp. 119–124, Feb. 2020.
[20] L. Liu, H. Chen, T. Hua, J. Mu, Z. Zhu, and Y. Yang, "A dual mode step-down switched-capacitor DC–DC converter with adaptive switch width modulation," *Microelectron. J.*, vol. 78, pp. 114–123, Aug. 2018.
[21] A. Veerabathini and P. M. Furth, "High-efficiency switched-capacitor DC–DC converter with three decades of load current range using adaptively-biased PFM," *J. Low Power Electron. Appl.*, vol. 10, no. 1, p. 5, Feb. 2020.
[22] S. Saini and D. S. Saini, "Power efficiency comparison for various MIM tile structures of fully integrated two-phase 2:1 SCVR for photovoltaic applications," *Opt. Laser Technol.*, vol. 186, Aug. 2025, Art. no. 112701.
[23] S. Bang, J.-s. Seo, L. Chang, D. Blaauw, and D. Sylvester, "A low ripple switched-capacitor voltage regulator using flying capacitance dithering," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 919–929, Apr. 2016.
[24] B. Zimmer, Y. Lee, A. Puggelli, J. Kwak, R. Jevtic, B. Keller, S. Bailey, M. Blagojevic, P.-F. Chiu, H.-P. Le, P.-H. Chen, N. Sutardja, R. Avizienis, A. Waterman, B. Richards, P. Flatresse, E. Alon, K. Asanovic, and B. Nikolic, "A RISC-V vector processor with simultaneous-switching switched-capacitor DC–DC converters in 28 nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 51, no. 4, pp. 930–942, Apr. 2016.
[25] H.-P. Le, S. R. Sanders, and E. Alon, "Design techniques for fully integrated switched-capacitor DC–DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.
[26] N. Butzen and M. S. J. Steyaert, "Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor DC–DC converters," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2843–2853, Dec. 2016.
[27] H. Kang, J. Jin, X. Liu, X. Wang, P. Hong, and J. Zhou, "A fully integrated multiphase switched-capacitor DC–DC converter with PFM control and charge sharing loss reduction," *Microelectron. J.*, vol. 108, Feb. 2021, Art. no. 104991.



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