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Design Considerations for Power-Efficient Fully Integrated 3:1 Switched Capacitor DC-DC Converter for PV Modules

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Abstract: This article presents a power-efficient DC-DC converter based on a switched-capacitor (SC) cell in power management systems supplied for fully integrated photovoltaic (PV) modules. These modules shall provide high-performance point-of-load voltage regulation. The primary objective of this study is to better utilize capacitance and switches by selecting a proper SC topology in order to improve the power efficiency of SC converters. A general steady-state performance model is investigated to optimize and compare a variety of SC DC-DC topologies. The investigation method relies on a charge-multiplier approach and considers the impact of area constraint on capacitors. To identify the most suitable topology for a given conversion ratio, the performance-limit metrics of SC converters are calculated. The analysis provides framework to determine optimum switch size and switching frequency for a two-phase 3:1 series–parallel converter for a target load current of 10 mA implemented on a 22 nm process technology. The results shows that a minimum of 250 MHz switching frequency is desirable for achieving a target efficiency greater than 85% while maintaining the minimum output voltage of 0.34 V. The analysis results are verified through MATLAB and PSpice-based simulations.

Keywords: charge-multiplier; performance metrics; steady-state analysis; switched-capacitor converter; topology comparison

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1. Introduction

In modern electronic products, the SC converter is a preferred choice for power conversion due to advantages like a reduced size, high efficiency, light weight, and high power density [1,2]. These converters are also known as charge-pump converters, as charges can either be delivered to or removed from the load. SC converters consist of switch capacitor arrays instead of bulky and noisy magnetic components (inductors), making them suitable for integrated circuit (IC) implementation, MIMO radar, and power management units (PMU) for photovoltaic (PV) modules [3]. The reduced module size for a fully integrated application that requires on-chip integration of passive components and PMU into a single sensor chip is shown in Figure 1 [4]. PV energy is one of the renewable energy sources that has many advantages due to its abundant supply and minimal maintenance requirements. The DC-DC converter regulates the constant output voltage under various operating conditions of PV cells. The performance of an SC converter is significantly affected by varying operational and environmental conditions, such as variation in PV module output characteristics and temperature fluctuations. The on-resistance of switches normally increases with a rise in temperature, resulting in higher conduction losses. In addition, there is a characteristic change in capacitors as well, like increased equivalent series resistance (ESR) that limits the overall performance of the converter. Further, the current–voltage (*I-V*) characteristics of PV modules deviate with changes in solar irradiance and temperature. The SC converter requires adapting to these variations by effectively

addressing these challenges in order to maintain steady output voltage, steady current, and optimum power delivery. The function of a DC-DC converter is to match the load to PV source, which adjusts the operating point and continuously regulates the voltage and current levels. PV cell's unregulated voltage is dynamically converted to a controlled DC output voltage using a DC-DC converter. A DC-DC converter with high efficiency is desirable for this conversion. To optimize the overall energy yield, integrated DC-DC converter modules can be developed as non-isolated types that are coupled independently for each PV module. Such modules are available in small packages with minimal external components that can operate with an extremely low quiescent current.

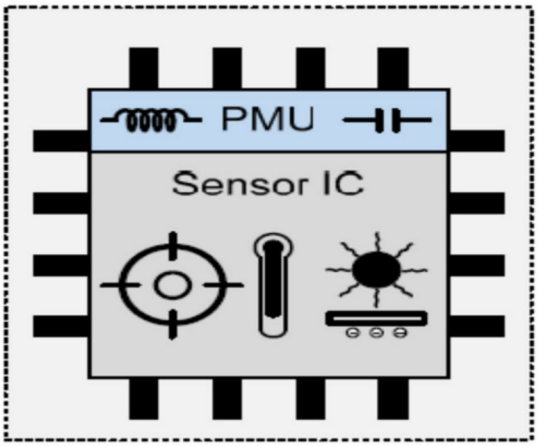

Figure 1. Fully integrated sensor module comprising PMU.

A high power density and suitability for small-scale integration result in the widespread use of SC converters. SC converters feature a variety of topologies, such as Ladder, Doubler, Fibonacci, Dickson, and Series–parallel. For the same number of switches and capacitors, Fibonacci and Doubler topologies deliver more voltage gain than other topologies. Ladder and Dickson topologies are employed for driver symmetry and power switching. However, there is a preference for Series–parallel architecture in order to maximize capacitor utilization without compromising performance [5]. Capacitor area and performance are the two important parameters that influence fully integrated SC converter implementations in today's CMOS technologies. Therefore, as the most favorable topology, Series–parallel is used to demonstrate the analysis and design technique in this work.

The steady-state behavioral model is designed to study specific characteristics of SC converters, such as the open-loop load line and conduction loss, by utilizing the concept of equivalent output resistance (R_{out}). The impedances in low- and high-frequency regions are called slow switching limit (SSL) impedance and fast switching limit (FSL) impedance, respectively, based on charge-multiplier vectors. The dominant losses for FSL and SSL impedances are switched conductive and capacitive losses. The limits for the total energy storage of capacitors and switch conductance are reached by optimizing components (switch and capacitor) size. This optimization method relies on the total device cost-based metrics defined in [6]. The reference [7] highlights the use of output impedance models to establish performance-limit merit for various SC topologies. These design methods allow for a comparison among several SC topologies, considering only conduction loss while neglecting switching and parasitic losses.

However, realistic converter designs involve losses beyond conduction, such as switching, gate-drive, and bottom-plate losses. Incorporating these additional factors ensures a more accurate representation of the converter's behavior, leading to more effective design and optimization strategies for improved efficiency and performance. The work presented in this paper investigates general steady-state performance models and develops performance-limit metrics for SC DC-DC converters. Built on an existing analysis of SC converters, the model is extended to determine the lowest possible power loss performance

metrics for efficiency enhancement, considering the impact of conduction, switching, and parasitic losses. We explored various methods to optimize and compare different SC DC-DC topologies that are valid in both SSL and FSL regions. The output impedances for the Ladder and Series–parallel topologies are compared in both asymptotic limits based on evaluated performance metrics to determine the best topology for a given conversion ratio.

The study is organized as follows: Section 2 provides a concise overview of the charge-multiplier approach and explains the steady-state performance modeling of a two-phase 3:1 SC DC-DC converter. Section 3 presents design considerations for efficiency enhancement of SC converters. In Section 4, performance-limit metrics are evaluated that are used to highlight the active-device and capacitance utilization of topologies. Section 5 provides the comparison results between Series–parallel and Ladder topologies of the SC DC-DC converter based on evaluated performance metrics. Finally, Section 6 concludes the paper.

2. A Review of Charge-Multiplier Model

In the literature, various analysis methods are presented for deriving converter's equivalent output impedance. Two basic methodologies have been explored extensively for modeling SC converters in general and power stages in particular: state-space modeling and averaging (steady-state) techniques. The first methodology focuses on manipulating equations; hence, it primarily utilizes numerical techniques. Alternatively, the charge-multiplier approach, which is based on similar circuit manipulations and uses an averaging technique, provides a single equivalent linear circuit model of the power stage, as illustrated in Figure 2. This has the unique benefit of offering the circuit designer an intuitive knowledge of the behavior of the original switched circuit and enabling the most efficient use of linear circuit analysis and synthesis tools in the design of regulators with switching converters [8]. This approach is adaptable for comparing different designs since it can be used systematically to any SC topology.

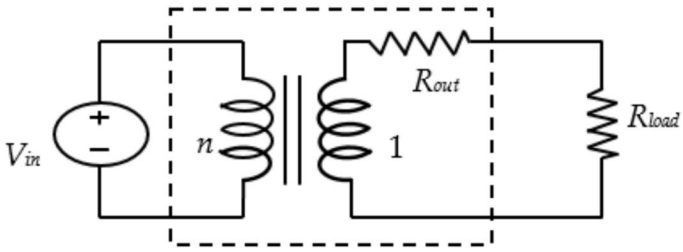

Figure 2. SCVR steady-state model.

The output impedance of a SC power converter determines its steady-state performance. Moreover, the converter offers an optimal DC voltage conversion ratio under no load and the voltage drop resulting from a non-zero load current manifests all the losses across R_{out}, as shown in Figure 2. Additionally, using the model shown in Figure 2, the ratio n, a rational number, defines the charge transfer (in a steady-state) between the input and output nodes [9]. The charge flow in each capacitor and switch is expressed as the output charge flow times a constant vector, denoted as a_c and a_r, referred to as a capacitor charge-multiplier vector and switch charge-multiplier vector, respectively.

Further, equations for the SSL and FSL impedances are derived using the concept of charge-multiplier vectors. It is possible to calculate a pair of charge-multiplier vectors, a^1 (phase1) and a^2 (phase2), for any standard two-phase SC converter. The charge flows that take place immediately following the switches are closed to initiate each phase of the SC circuit and are represented by the charge-multiplier vectors. According to [10], the KCL constraints in each topological phase can be used to uniquely compute the charge-multiplier vectors. Every component of a charge-multiplier vector reflects the charge flow (in each phase) into a particular capacitor/switch (q_n^1) or independent voltage source, normalized with respect to the output charge flow (q_{out}) as follows:

$$a^1 = \left[q_{out}^1\ q_1^1 \ldots q_n^1\ q_{in}^1\right] / q_{out} \quad (1)$$

An SC converter operates in three different regions, namely low frequency, high frequency, and intermediate regions, when the sub-circuit time constant (τ_i) is compared with the switching period (T_s). The two asymptotic limits, namely the SSL and FSL, are used for a performance analysis of SC converters and have generalized forms of $\tau_i << T_s$ for the SSL and $\tau_i >> T_s$ for the FSL, respectively. An empirical approximation is given for the intermediate region of operation using corner frequency. Paper [11] suggested a method built on the investigation of switch power loss to develop a generalized model for the FSL equivalent output impedance of the converter. Afterward, the expressions for converter output impedance are available for the full switching frequency range.

In an SSL analysis, all resistive components, like switch resistances, are assumed ideal, while other parasitic losses related to flying capacitors, like equivalent series resistances (ESR), are ignored [12]. The output impedance related to the SSL is given as follows:

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_i \frac{(a_{c,i})^2}{C_i f_{sw}} \quad (2)$$

In (2), the capacitance of an ith capacitor is denoted by C_i, $a_{c,\,i} = q_{in}/q_{out}$ represents the ith value of capacitor charge-multiplier vector (a_c), and f_{sw} is the converter switching frequency of operation. The output impedance related to the FSL is expressed as follows:

$$R_{FSL} = 2\sum_i R_{on,i}(a_{r,i})^2 \quad (3)$$

where $R_{on,\,i}$ is the ith switch on-resistance and $a_{r,\,i}$ is the ith value of charge-multiplier vector (a_r) of a switch. In (2) and (3), all other conductive interconnects were ignored, and a switching duty cycle value was assumed to be 50%. This method is simpler than the earlier one suggested in [13], as it considers active and passive elements, namely switches and capacitors, independently. Further, an SC converter is modeled by employing coupled charging loops, as in the case of Ladder topology, and there is no need to search for RC sub-circuits. Therefore, this modeling procedure is used to implement complex SC converters, as it neglects resistive loss in the SSL and considers only switch conduction loss in the FSL. During FSL calculation, the flying capacitors' ESR is utilized, and the converter output impedance for the intermediate frequency range is revised using a new expression based on the Minkowski distance formula [14], given as follows:

$$R_{out} \approx \sqrt[i]{R_{SSL}^i + R_{FSL}^i} \quad (4)$$

Further, R_{out} calculations are more precise for i value 2.54514 instead of 2. This value of i modifies the expressions presented in [6], where the calculations are performed for i equal to 2. Since the outcome was determined empirically through hypothesis and validation, the overall precision for the complete frequency range remained uncertain.

2.1. Modeling of 3:1 Series–Parallel SC Converter

The Series–parallel 3:1 step-down converter, as illustrated in Figure 3a is used to describe the basic working of SC converters. Each switch in the converter operates at a 50% duty cycle with two phases known as φ_1 and φ_2, respectively. The converter operates between two modes (common and gain) by turning the switches on and off during each phase [15]. There is a total of seven switches in a single-phase 3:1 SC converter, in which four SW_2, SW_3, SW_5, and SW_6 operate in gain mode and the remaining three SW_1, SW_4, and SW_7 operate in common mode, as shown in Figure 3b.

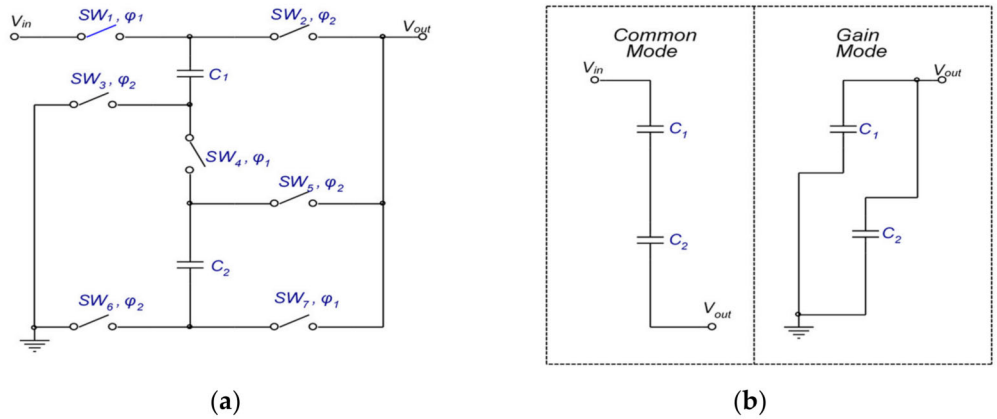

Figure 3. 3:1 Series–parallel SC converter. (**a**) Schematic. (**b**) Modes of operation: common mode (φ_1) and gain mode (φ_2).

In φ_1, the flying capacitors (C_{fly}/C_1 and C_2) are charged to input potential while connected in series with the input. In φ_2, also known as the discharging phase, C_{fly} transfers the charge to the load, resulting in 1/3 gain since the output voltage is equivalent to one-third of the supply voltage. For the calculation of SSL output impedance, the charge-multiplier vector for capacitors (taken as a single phase due to charge conservation principle) is given as follows:

$$a_c = [\ 1/2\ \ 1/2\ ] \tag{5}$$

Using (2), the SSL impedance is calculated as follows:

$$R_{SSL} = \frac{1}{2C_{fly}f_{sw}} \tag{6}$$

The total R_{SSL} will be half of the earlier (which is for a single-phase) in the case of a two-phase 3:1 Series–parallel converter, given as follows:

$$R_{SSL} = \frac{1}{4C_{fly}f_{sw}} \tag{7}$$

For the calculation of FSL output impedance, the charge-multiplier vector for switches in both phases (common and gain) is given as follows:

$$a_r = [\ 1/2\ \ 1/2\ \ \ 1/2\ \ \ 1/2\ \ \ 1/2\ \ \ 1/2\ \ \ 1/2\ ] \tag{8}$$

Using (3), the FSL impedance is calculated as follows:

$$R_{FSL} = 2\,^{7}/_{4}\ R_{on} \tag{9}$$

As in the case of the R_{SSL} calculation, the R_{FSL} value is also reduced to half in the case of a two-phase 3:1 Series–parallel converter as the resistances (in two phases) are connected in parallel. Therefore, the total R_{FSL} given by

$$R_{FSL} = {}^{7}/_{4}\ R_{on} \tag{10}$$

2.2. Modeling of 3:1 Ladder SC Converter

A single-phase Ladder converter having a conversion ratio of 3:1 is presented in Figure 4. It comprises two sets (Ladder) of capacitors known as DC-referenced capacitors and flying capacitors (C_{fly}). The first set of capacitors are charged to supply voltage (DC) equal to the ratio of the integer multiple of the input voltage and the denominator of the conversion ratio. While the remaining set of C_{fly} transfers the charge from DC-referenced

capacitors to equalize them [16]. Further, the switches are turned on and off in alternate phases for establishing a connection between DC-referenced capacitors and C_{fly}.

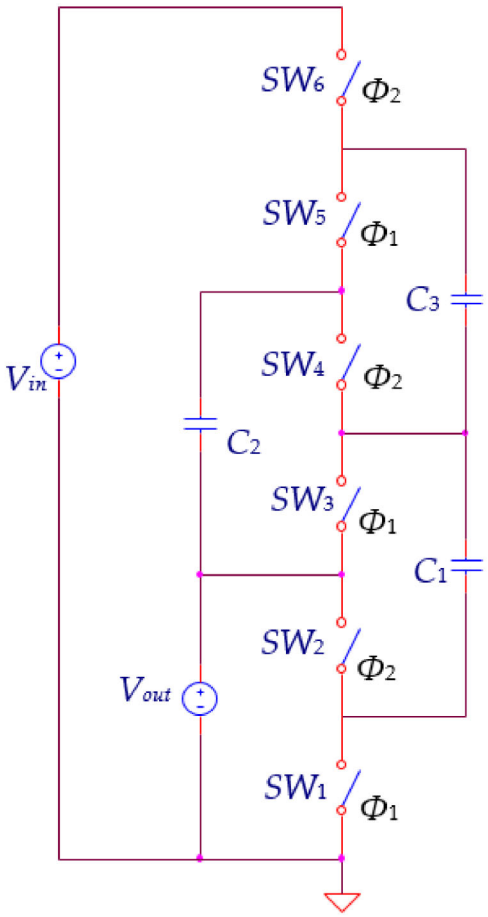

Figure 4. A 3:1 SC Ladder converter circuit.

Initially, the two-phase network is drawn excluding the switches from circuit configuration in different phases. Further, charge-multiplier vectors of capacitors between input and output points are calculated for each node. As depicted in Figures 5 and 6, the converter operates in two phases, φ_1 and φ_2, respectively. To evaluate the charge flow through capacitors, KCL and multi-step methodology is used [17].

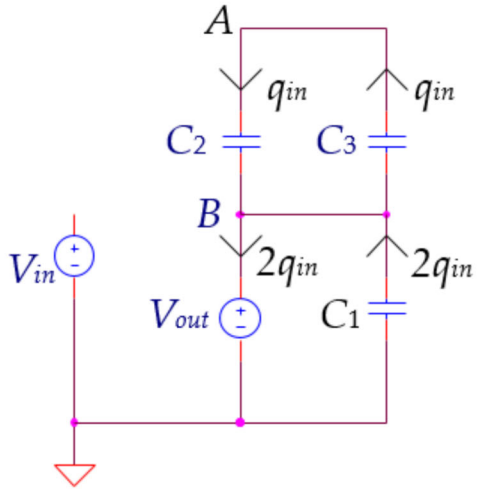

Figure 5. Capacitor charge flow for 3:1 Ladder converter in phase1 (φ_1).

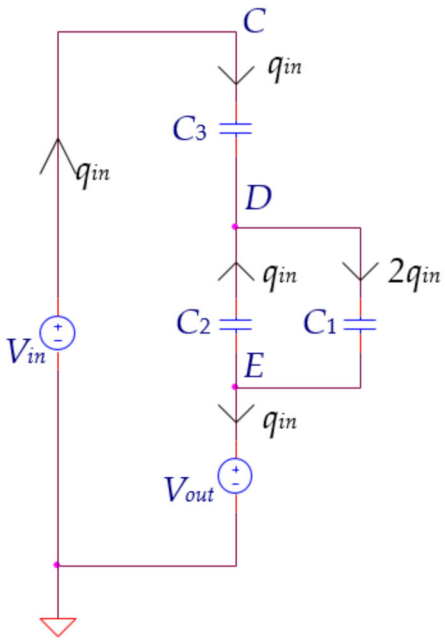

Figure 6. Capacitor charge flow for 3:1 Ladder converter in phase 2 (φ_2).

In a steady-state performance analysis, the charge flow in each phase follows the charge conservation principle, making the charge flow through capacitors in φ_1 equal and opposite to that of φ_2. In the example circuit shown in Figures 5 and 6, applying KCL at each node leads to the following:

- Phase 2: node C yields $q^2_{c4} : q^2_{c4} = +q_{in}$;
- Phase 1: node A yields $q^1_{c3} : q^1_{c3} = -q^1_{c4} = +q_{in}$;
- Phase 2: node D yields $q^2_{c2} : q^2_{c2} = -q^2_{c4} - q^2_{c3} = -2q_{in}$;
- Phase 1: node B yields $q^1_{out} : q^1_{out} = +2q_{in}$;
- Phase 2: node E yields $q^2_{out} : q^2_{out} = +q_{in}$.

The output charge $q_{out} = q^1_{out} + q^2_{out}$ (in both phases) is equal to the input charge multiplied by three. Therefore, the input charge flow is equal to one-third of q_{out}, which depicts the charge conservation for the 3:1 conversion ratio. Therefore, the capacitor charge vector given as follows:

$$a_c = [\, 1/3 \;\; -1/3 \;\; 2/3 \,] \tag{11}$$

Due to charge conservation, the charge multipliers of capacitors in two phases are equal and opposite, such that $a_c = a^1_c = -a^2_c$ [6]. Hence, a single charge-multiplier vector of the capacitor is defined. Further, the R_{SSL} in (1) is simplified as (11) for the given values of C_{fly} and f_{sw}, as follows:

$$R_{SSL} = \frac{2/3}{C_{fly} f_{sw}} \tag{12}$$

When the charge multipliers of the capacitors are calculated, the switches are included in the network. For the two networks shown in Figures 7 and 8, the orientation of charge flowing through each closed switch is labeled. After identifying each closed switch charge flow using KCL constraints, the switch charge-multiplier vector for the 3:1 Ladder circuit is calculated as follows:

$$a_r = \begin{bmatrix} a^1_{r1} \\ a^2_{r2} \\ a^1_{r3} \\ a^2_{r4} \\ a^1_{r5} \\ a^2_{r6} \end{bmatrix} = \begin{bmatrix} -2/3 \\ -2/3 \\ 1/3 \\ 1/3 \\ 1/3 \\ 1/3 \end{bmatrix} \tag{13}$$

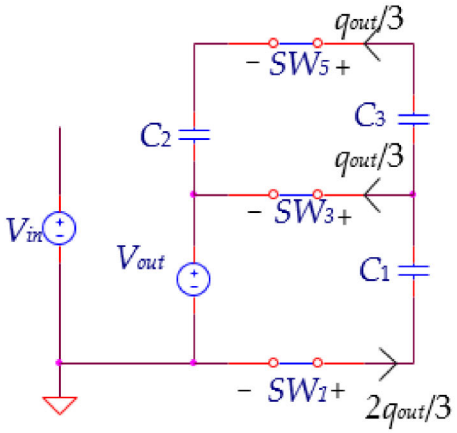

Figure 7. Switch charge flow for 3:1 Ladder converter in phase 1 (φ_1).

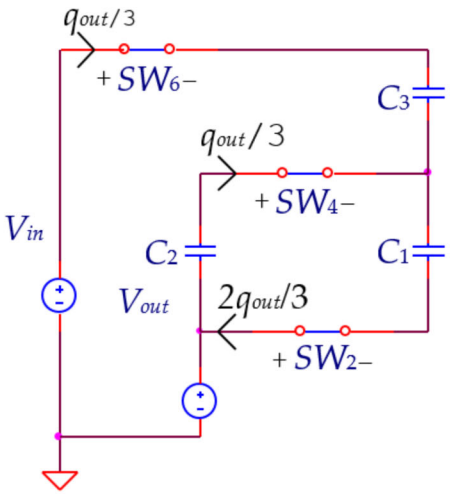

Figure 8. Switch charge flow for 3:1 Ladder converter in phase2 (φ_2).

If the switch blocks positive voltage in φ_1, then negative current will flow in φ_2, resulting in a negative value of the charge-multiplier vector. For a given value of R_{on}, R_{FSL} is calculated using (3), given as follows:

$$R_{FSL} = {}^{4}/_{3} R_{on} \tag{14}$$

3. Design Considerations (Loss Model)

In general, an SC converter has several components that contribute to the power loss in various parts of the circuit. Assuming ideal switches with constant on-resistance simplifies the steady-state analysis of an SC converter. On the other hand, non-idealities, such as variable resistance and leakage, can significantly affect the performance of a converter. During conduction, larger voltage drops across the switches due to variation in voltage levels and temperature may result in power losses that are higher than anticipated. Furthermore, in energy-sensitive designs like PV systems, leakage currents through non-ideal switches can affect the effective output voltage and current provided to the load, especially under low-load conditions. This can result in less efficient energy conversion. To enhance the efficiency of a converter, the impact of these components need to be minimized [18]. The overall power loss depends upon the following parameters:

- R_{SSL} loss;
- R_{FSL} loss;
- MOSFET parasitic capacitance (C_{SW}) loss;
- Bottom-plate capacitance (C_{bott}) loss;

- ESR loss.

3.1. Proposed Two-Phase 3:1 Series–Parallel SC Converter Operation

An SC converter transmits the charge from input to the load with the help of flying capacitors switching between a series and parallel configuration, which act as fixed voltage sources. To demonstrate the loss analysis and design parameter computation, Figure 9 represents a two-phase 3:1 Series–parallel SC DC-DC converter. There are four flying capacitors, C_1, C_2, C_3, and C_4, in the network.

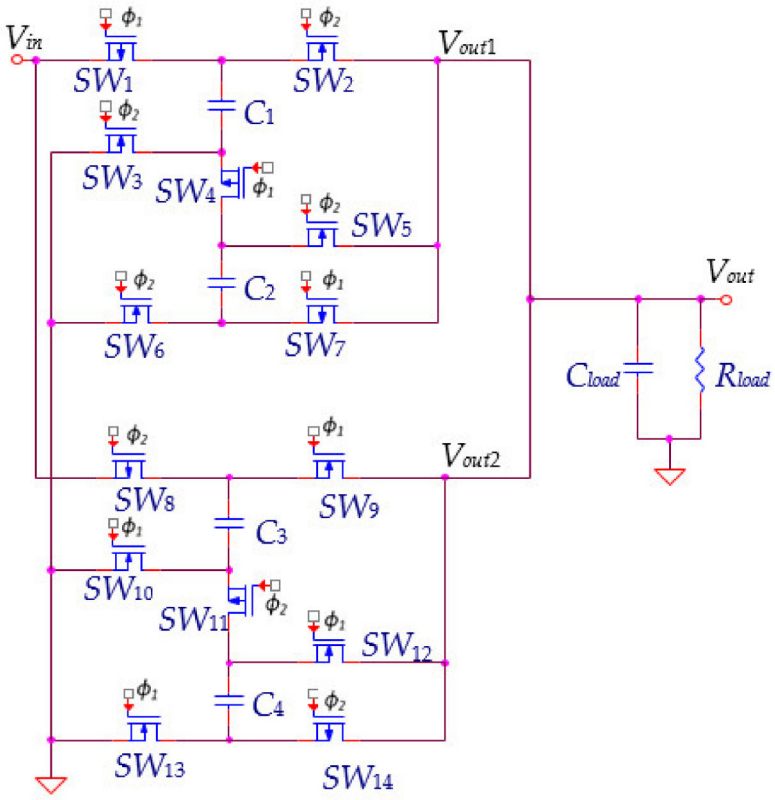

Figure 9. Two-phase 3:1 Series–parallel SC converter schematic.

A non-overlapping clock controls the switching activity of capacitors between two phases. Flying capacitors charge and discharge as the switching clock operates through fourteen switches [19]. Out of these fourteen switches, seven are conducting in φ_1, and the remaining seven are conducting in φ_2, as shown in Figure 9. While capacitors C_1 and C_2 are connected in series in φ_1 and charged from the input source, the capacitors C_3 and C_4 are in a parallel configuration and discharging through the load. Further, the capacitor operation is interchanged in φ_2. To reduce the output voltage ripples, a load capacitor (C_{load}) is used.

3.2. Loss Model Including Parasitic

An SC converter performance suffers from the various parasitic elements linked to MOSFET transistors (act as switches) [20]. There are three main losses related to transistors, namely C_{gs} (gate to source), C_{ds} (drain to source), and C_{gd} (gate to drain) capacitances, respectively. The conductance (or area) of the switches and f_{sw} are directly correlated with these losses. The gate capacitance ($C_{sw} = C_{gs} + C_{gd}$) is the main cause of the parasitic loss, as shown in Figure 10.

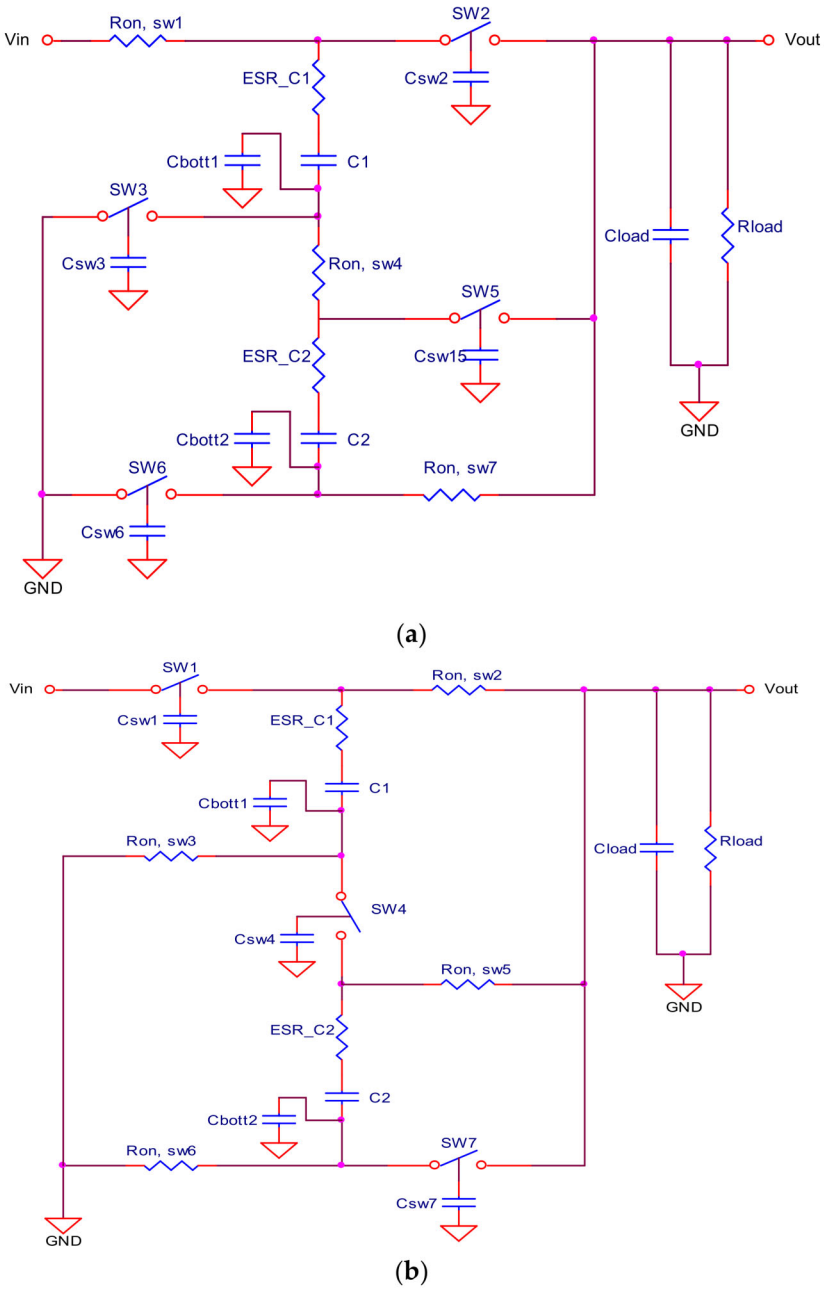

Figure 10. Two-phase operation of 3:1 Series–parallel converter, including parasitic C_{sw}, C_{bott}, and R_{esr}. (**a**) Phase 1: φ_1; (**b**) phase 2: φ_2.

The SSL impedance is determined by choosing the proper values for the C_{fly} and f_{sw} using (7). Similarly, by selecting suitable values for R_{on}, the FSL impedance can be calculated using (10). Since the direct addition provides a value higher than the expected one, the corresponding impedance is calculated as the quadratic sum of R_{SSL} and R_{FSL}. Thus, the R_{out} is given as follows:

$$R_{out} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{15}$$

The loss associated with SSL and FSL impedances is known as conduction power loss (P_{RES}). The SSL power loss $\left(P_{loss,SSL}\right)$ is determined as follows:

$$P_{loss,SSL} = I_{out}^2 R_{SSL} \tag{16}$$

Similarly, FSL power loss $\left(P_{loss,FSL}\right)$ is calculated as follows:

$$P_{loss,FSL} = I_{out}^2 R_{FSL} \tag{17}$$

Hence, the total P_{RES} is represented as

$$P_{RES} = \sqrt{\left(P_{loss,SSL}^2\right) + \left(P_{loss,\ FSL}^2\right)} \tag{18}$$

The conduction (P_{RES}) and switching (P_{sw}) power losses are used to approximate an SC converter's efficiency. An equivalent output impedance corresponding to both losses is computed for a target load current (I_{out}). Further, P_{sw} occurs mainly due to parasitic capacitances associated with switches and flying capacitors, namely C_{sw}, C_{bott}, and ESR. For every clock cycle, the charging and discharging of these parasitic capacitances keep adding to undesired power loss in the converter. The C_{bott} is generally fixed for a given capacitor technology [21]. Therefore, the total parasitic capacitance and voltage swing at a particular node used to estimate the total P_{sw} is given as follows:

$$P_{sw} = P_{loss,swcap} + P_{loss,bottcap} + P_{loss,esr} \tag{19}$$

The energy needed to turn on and off the gates of power devices, such as MOSFETs, also contributes to gate drive losses. The gate charge and operating frequency are taken into account while calculating these losses. The power loss caused by switch-parasitic capacitance is expressed as follows:

$$P_{loss,swcap} = N_s f_{sw} C_{sw} V_{sw,cap}^2 \tag{20}$$

In (20), the variables f_{sw}, C_{sw}, N_s , and V_{sw} represent switching frequency, switch-parasitic capacitance, the number of switches (corresponds to the switch size), and switch-blocking voltage, respectively. For a two-phase 3:1 SC converter, the total power loss is fourteen times higher compared to the single-switch capacitor loss, as there are a total of fourteen switches in the circuit configuration shown in Figure 9. Similarly, the switching power loss resulting from bottom-plate capacitance is calculated as follows:

$$P_{loss,bottcap} = N_C f_{sw} C_{bott} V_{cap}^2 \tag{21}$$

Regarding the flying capacitor's C_{bott} and its voltage, V_{cap}, N_C is the number of capacitors (corresponds to capacitor area) given in (21). In certain circuit configurations, the capacitance connected to the bottom-plate of the flying capacitor is the source of bottom-plate capacitance loss. The impact on efficiency depends on the operating frequency and the amount of current flowing through the flying capacitors. Flying capacitor ESR reduces efficiency by producing heat during operation, especially in cases with high loads and significant current. The power loss resulting from ESR is given as follows:

$$P_{loss,ESR} = I_{out}^2 R_{ESR} \tag{22}$$

In (22), the variables R_{ESR} and I_{out} represent flying capacitor ESR and converter output current, respectively, as shown in Figure 10. The overall power loss (P_{loss}) of an SC converter is equivalent to the sum of P_{sw} and P_{RES}, given as

$$P_{loss} = P_{RES} + P_{sw} \tag{23}$$

This new model is efficient for the performance modeling and designing of SC converters, where the impact of parasitic loss is also considered. A precise operating point is selected to achieve low switching losses while maintaining the smallest possible value of equivalent output impedance. The output power (P_{out}) is given as follows:

$$P_{out} = \frac{V_{out}^2}{R_{load}} \tag{24}$$

In (24), the variables V_{out} and R_{load} represents the nominal output voltage and load resistance, respectively. Further, the actual output voltage ($V_{o,real}$) at the load is obtained through the voltage-division method, calculated as follows:

$$V_{o,real} = V_{out} \frac{R_{load}}{(R_{load} + R_{out})} \tag{25}$$

The efficiency *(η)* of the two-phase 3:1 converter operating in a Series–parallel configuration is given by the following:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \tag{26}$$

To determine the optimum efficiency for an SCVR design that is limited by area, there is a requirement to minimize losses.

$$\eta_{opt} = \frac{P_{out}}{P_{out} + P_{loss,\,min}} \tag{27}$$

In (27), $P_{loss,\,min}$ is the corresponding conversion power loss, including conduction, switching, and parasitic loss. Using the Matlab optimization function, namely 'fmincon', the minimum power loss is calculated for different load currents and flying capacitance values using an interior-point algorithm. A DC-DC converter efficiency is significantly affected by the switch size (or area), which influences both switching and conduction losses. In general, a lower on-resistance is achievable with a larger switch area, which improves operational efficiency by minimizing conduction losses. Additionally, if the switch size (N_s) is too small, it may exhibit greater parasitic capacitances, which results in higher switching losses during turn-on and turn-off transitions. Optimizing both cost and performance elements involves finding an appropriate switch size. Figure 11 shows efficiency variation with switch size (area) under a varying load current of the proposed SC converter operating at 250 MHz switching frequency. The curves presented are generated by varying the switch area and subsequently measuring the efficiency of the converter across different load conditions.

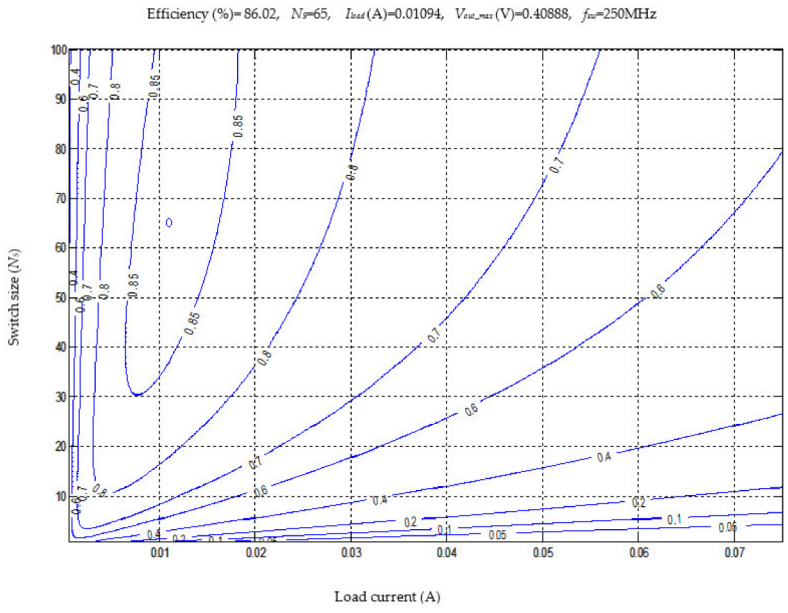

Figure 11. Efficiency variation with number of switches (N_S) and I_{load} (A) for f_{sw} equal to 250 MHz.

Hence, the optimal efficiencies for the 3:1 SC converter are obtained using (27). The contour plot of the 3:1 SC converter operating at 250 MHz switching frequency is shown in Figure 11, which represents the optimal efficiency. At an output voltage of 0.40 V and 10 mA load current, the maximum efficiency of 86.49% is attained, which corresponds to an N_s value of 65 equivalent to R_{on} of value 0.76 Ω (of unit cell). Further, it follows that a minimum 250 MHz switching frequency is required for achieving a target efficiency and output voltage greater than 85% and 0.34 V, respectively.

4. Development of Performance-Limit Metrics

Using the proposed methodology, design steps were followed to reach a specific operating point that maximize efficiency. Most SC converters operate at optimum efficiency when they have a low MOSFET resistance and large capacitance. Hence, the performance tradeoff exists between f_{sw} and switch size (N_S) parameters for a specific efficiency. For a fixed f_{sw}, the increase in N_S leads to reduction in P_{RES} and an increase in P_{sw} due to increased switch-parasitic capacitance and vice versa. Similarly, for fixed N_S, the decrease in f_{sw} leads to increase in P_{RES} and a reduction in P_{sw} and vice versa [22]. Therefore, the optimal f_{sw} and N_S is essential. In this paper, MATLAB simulation was used to determine the optimal f_{sw} and N_S by segmenting the switch into multiple regions. For every region, the f_{sw} corresponding to maximum efficiency was calculated. The N_S region with the maximum efficiency was chosen, as shown in Figure 11.

In this section, the two most commonly used topologies, namely Ladder and Series–parallel, were examined for a 3:1 conversion ratio. Further, the two types of performance metrics, namely the SSL and FSL, of SC converter for 3:1 conversion ratio were derived in this section. These matrices were calculated as the ratio of Volt–Ampere (*V-A*) product of each converter and the sum of Switch Conductance–Volt square (G-V^2) products of its sub-components. At a lower conversion ratio (2:1), most converters are modeled into a Doubler structure, with single stage having the same metric [23]. However, converters differ significantly at higher ratios in terms of steady-state performance. Since the topologies comparisons are not dependent upon technology and implementation, therefore, the performance metrics were evaluated based on component optimization using *V-A* product of each component. These performance metrics relate the converter power to the device metrics based on total *V-A* product of components, namely one for the SSL impedance calculation and the other for the FSL output impedance calculation. In SC converters, the power consumption is inversely related to its equivalent output impedance and directly related to the square of output voltage for constant output impedance. Therefore, the converter power handling capability is represented by its G-V^2 product. The SSL performance metric (M_{SSL}) is calculated as follows:

$$M_{SSL} = \frac{V_{o,real}^2 / R_{SSL}}{f_{sw} \sum_{i \epsilon caps} C_i v_{c,i}^2 / 2} \tag{28}$$

In (28), the variables $V_{o,real}$ and R_{SSL} represents the converter's actual output voltage and optimized SSL impedance, respectively. The performance metric's denominator is calculated as the product of converter frequency with the total energy stored in network capacitors. On similar lines, the FSL performance metric (M_{FSL}) is given as follows:

$$M_{FSL} = \frac{V_{o,real}^2 / R_{FSL}}{\sum_{i \epsilon switches} G_i v_{r,i}^2} \tag{29}$$

In (29), R_{FSL} denotes optimized resistive output impedance in the FSL region of operation. The denominator represents the sum G-V^2 products of switches. The optimized performance metrics, evaluated based on minimum power loss using charge-multiplier vectors and components (switch and capacitor) blocking voltage [24], is given as follows:

$$M_{SSL} = \frac{4V_{o,real}^2}{\left(\sum_{i\epsilon caps} v_{c,i(rated)} \sqrt{\sum_{j=1}^{n} \left(a_{c,i}^{j}\right)^2}\right)^2} \tag{30}$$

$$M_{FSL} = \frac{V_{o,real}^2}{n\left(\sum_{i\epsilon sw} v_{r,i(rated)} \sqrt{\sum_{j=1}^{n} \left(a_{r,i}^{j}\right)^2}\right)^2} \tag{31}$$

Further, the two-phase converters are examined for the comparison of Ladder and Series–parallel topologies. Hence, both the SSL and FSL metrics are simplified for two-phase configuration, as given below:

$$M_{SSL} = \frac{2V_{o,real}^2}{\left(\sum_{i\epsilon caps} \left|a_{c,i} v_{r,i(rated)}\right|\right)^2} \tag{32}$$

$$M_{FSL} = \frac{V_{o,real}^2}{2\left(\sum_{i\epsilon sw} \left|a_{r,i} v_{r,i(rated)}\right|\right)^2} \tag{33}$$

where $V_{o,real}$ is given by (25). Further, the impedances for both topologies are given as follows:

- Series–parallel topology:

$$R_{SSL1} = \frac{1}{4\ C\ f_{sw}\ N_C} \tag{34}$$

$$R_{FSL1} = \frac{7\ R_{on}}{4\ N_S} \tag{35}$$

- Ladder topology:

$$R_{SSL2} = \frac{1}{3\ C\ f_{sw}\ N_C} \tag{36}$$

$$R_{FSL2} = \frac{4\ R_{on}}{3\ N_S} \tag{37}$$

Substituting Equations (34)–(37) in (15), we derive the corresponding R_{out} that is used to calculate the actual $V_{o,real}$ using (25). Further, these units with less metrics given in (32) and (33) are used for comparison of different topologies for switch-limited and capacitor-limited design spaces. Hence, these matrices are considered ideal for performance comparisons of converter topologies. The converter with the highest performance metric gives superior performance. In Section 5, a comparison of two performance metrics on a logarithmic scale is given for both topologies.

5. Simulation Results

To demonstrate the proposed methodology analyzed in this work, the MATLAB simulation results are obtained for a two-phase 3:1 Series–parallel SC converter using four flying capacitors. The basic circuit (unit-cell) comprises fourteen switches and four flying capacitors, resulting in the two-phase structure of the converter, as shown in Figure 9. Further, the flying capacitors (C_{fly}: C_1, C_2, C_3, and C_4) are realized as MIM capacitors for better capacitance utilization (area) for enhanced power efficiency. Although MIM capacitors have reduced capacitance density compared with MOS, they are considered the most appropriate solution for fully integrated circuits, as they provide nearly ten times lower bottom-plate capacitance and are also available in a standard CMOS process. We have used the approach given in Section 3.2 to determine the capacitor and switch size.

The maximum efficiency is calculated for optimum switch size and switching frequency as shown in Figure 11.

The 22 nm SoC process technology parameters utilized in the converter's design are listed in Table 1. An input voltage of 1.24 V is considered. For the target V_{out} of 0.34 V, the R_{load} of 34 Ω is calculated as equivalent to 10 mA load current. The expression for the on-resistance (R_{on}) of a switch is (K_R/W), where W is the switching device's width and K_R [Ω-µm] is dependent on the switch type (PMOS or NMOS) [14]. When considering PMOS/NMOS switch sizes of 0.48 µ/0.03 µ @110 °C, a V_{GS} of 0.9 V and an R_{on} value of 50 Ω are determined. Further, PSpice is used to examine the performance for the various primary switch value (R_{on}). It is preferable to have smaller switches in order to reduce the amount of charge injection and clock feedthrough that arise from the overlap capacitance present in switches. C_{sw} accounts for the total gate capacitance for each switch. Flying capacitors C_1, C_2, C_3, and C_4 are considered as 0.4 nF each, while C_{bott} is calculated as 0.4 pF, which is equal to the ratio of flying capacitance divided by a constant (C_{fly}/constant), where the constant is equal to 1000.

Table 1. Technology parameters.

Input Parameter	Value
V_{in}	1.24 V
Ideal ratio	1/3
R_{load}	34 Ω
R_{on} of the unit switch cell	50 Ω
C_{sw}	10 fF
C_{fly}	0.4 nF
C_{bott}	C_{fl} constant
ESR (for C_{fly})	0.2 Ω

There are various practical challenges with integrating 22 nm process technology into power-efficient designs, such as a fully integrated 3:1 switching capacitor DC-DC converter. Power density rises with decreasing transistor sizes, producing a large amount of heat. Further, leakage currents become a major issue at smaller nodes, affecting total power efficiency. Parasitic capacitances of 22 nm have the potential to significantly influence signal integrity, especially in high-frequency applications. These issues have an impact on scalability since they make it more challenging to attain the required performance and efficiency in practical applications.

For capacitance modeling, a MIM capacitor of 0.4 nF is considered for each flying capacitor C_1, C_2, C_3, and C_4, resulting in a total capacitance value of 1.6 nF, as shown in Table 2. PSpice simulations are conducted with the actual extracted netlist of the MIM capacitor, including the switch and pre-driver parasitic. The frequency response of MIM tile structure is presented in Figure 12.

Table 2. Capacitance modeling parameters.

Element	No. of Elements	Values
Total No. of phases	2	-
Total No. of MIM capacitor	4	0.4 nF (each), 1.6 nF (total)
MIM capacitor per phase	2 (1 for each C_{fly})	0.4 nF (for each C_{fly})
Tile cap value	96 (=1.6 nF capacitance)	16 pF
Equivalent ESR for 1.6 nF @ 250 MHz	-	0.2 Ω

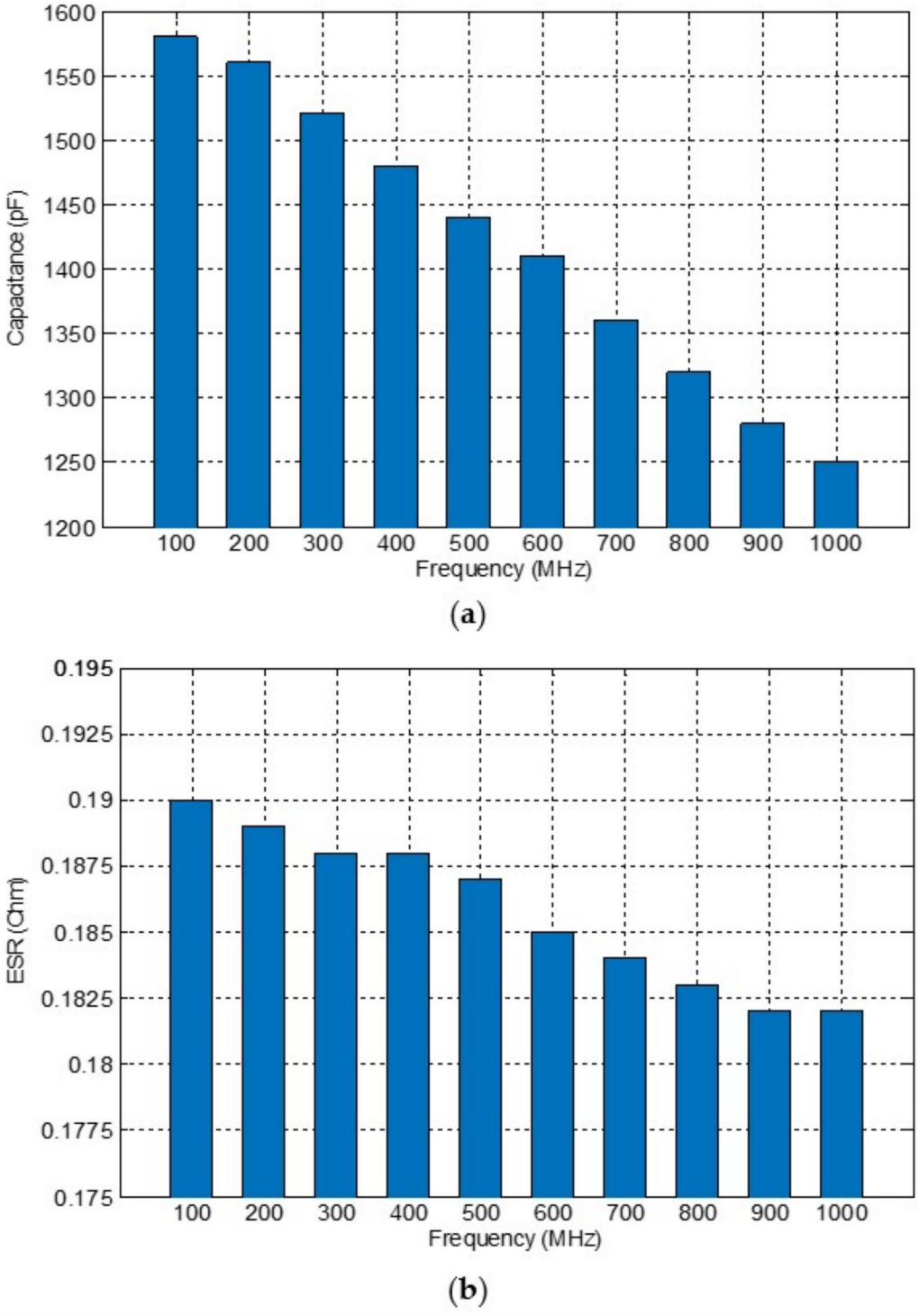

Figure 12. Frequency response of MIM capacitor: (**a**) capacitance and (**b**) ESR variation with switching frequency of operation.

SC DC-DC converter applications can benefit from integrated capacitors for low power applications, and there are many design considerations specific to each capacitor technology. The initial step in a typical design process would be to determine the charge multipliers for the desired SC topology. Additionally, capacitors are chosen based on the SSL impedance, which is the output impedance that is related to the capacitors. To ensure the best possible utilization of devices, a cost-based constraint is applied to the capacitor optimization. Understanding the working voltages of the components is necessary for this operation. The constraint most precisely reflects physical size (area) and cost because the total energy

storage of all capacitors was kept constant, as indicated by Etot. This constraint is calculated as follows:

$$\sum_{iecap} \frac{1}{2} v_{c,i(rated)}^2 c_i = E_{tot} \quad (38)$$

where C_i and $V_{c,i}$ represents the capacitance and rated voltage of ith capacitor, respectively. The capacitor's rated voltage determines its size and cost, not the maximum voltage it experiences when in use, which in turn affects how much energy it can store. Further, the operating voltage of the capacitor must be lower than its rated value to prevent damage to the component. It should also be closer to the rated voltage in order to maximize the device's utilization. These design techniques significantly improve the performance (efficiency) of an SC converter, particularly if it has a high conversion ratio. Further, the $I_{load,max}$ of 5 mA per phase is taken based on power density considerations, resulting in a target I_{load} of 10 mA for a two-phase 3:1 SC converter, as the target I_{load} is equal to two times the I_{load} per phase.

The variation of maximum attainable efficiency and switching frequency with capacitance for N_S equal to 65 (R_{on} = 50/65 Ω), respectively, is shown in Figure 13. For a given output impedance, the switch silicon area and capacitor energy storage can be used more effectively by using the optimization approaches described below. First, the SSL impedance is inversely proportional to the capacitance; hence, an increase in capacitance results in decreased R_{SSL} impedance. Moreover, f_{sw} decreases as C_{fly} increases, which reduces parasitic loss and eventually leads to enhanced efficiency. The parasitic device (described in Section 3.1) determines the maximum feasible f_{sw} depending on the process technology used to implement the SC converter. Efficiency improves due to lower parasitic losses resulting from lower switching frequencies, as shown in Figure 14. The optimal frequency balances conduction losses (which decrease with a higher frequency due to a smaller ripple) and switching losses (which increase with frequency). Higher load currents generally favor lower frequencies to reduce switching losses. Advanced nodes allow for higher frequencies due to lower parasitic capacitances. Moreover, it offers significant efficiency improvements but at a higher cost and design complexity.

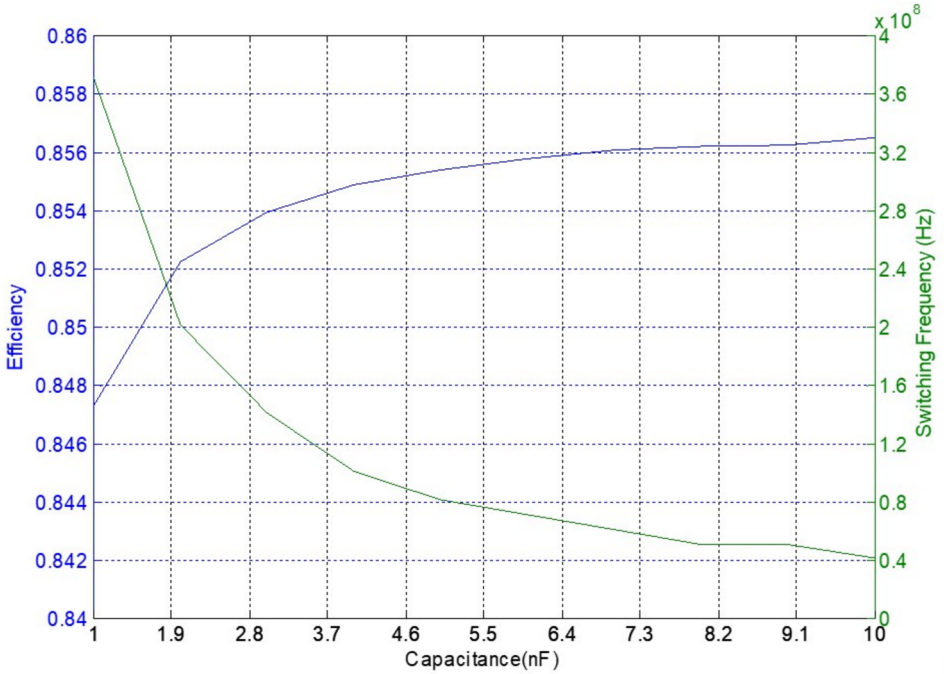

Figure 13. Efficiency and switching frequency variation with capacitance.

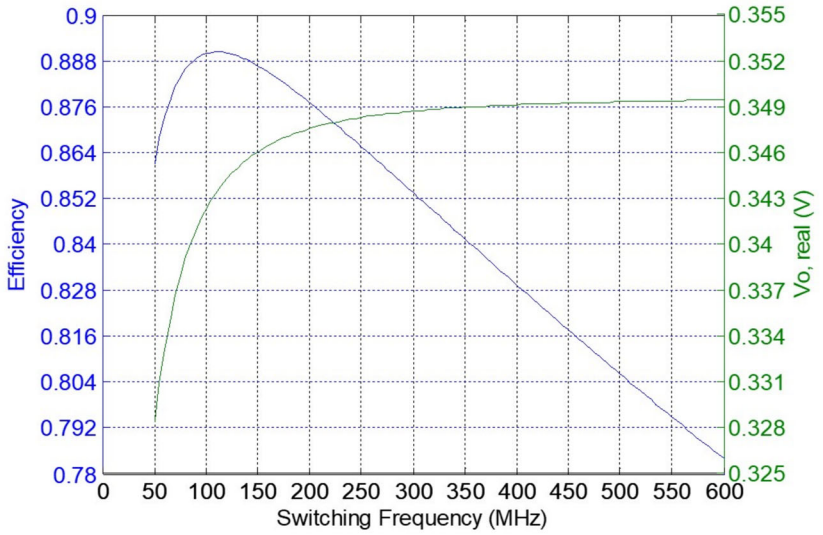

Figure 14. Efficiency and output voltage tradeoffs with varying switching frequency for N_s = 65 (R_{on} = 0.76 Ω) and ESR = 0.2 Ω.

The same total G-V^2 constraints remain valid for fully integrated applications provided the nominal voltage and transistor length (L) scale in accordance with process generations. Advanced nodes generally allow for lower R_{on} and C_{sw} per unit width. Hence, it results in a reduction in switch size for the same performance. To increase the switch conductivity (G), many blocks of switches are connected in parallel. Further, the converter design employing MIM capacitors can greatly improve light load efficiency by varying the MOSFET width (W). Figure 15 illustrates how efficiency changes as switch size (N_s) increases. The optimal switch size balances conduction losses and switching losses. It is highly sensitive to load current variation, as higher load currents favor larger switches to reduce conduction losses for optimal efficiency. Furthermore, performance does not considerably increase at higher values of N_s because switch gate parasitic loss becomes dominant at these values. As N_s increases, the equivalent switch resistance, or R_{on}/N_s, decreases; thereby, increasing switch conductance finally results in enhanced efficiency. Figure 16 shows the variations in V_{out} and efficiency with different load resistances (R_{load}). For R_{load} ranges from 25 Ω to 50 Ω, the converter efficiency increases to 85%.

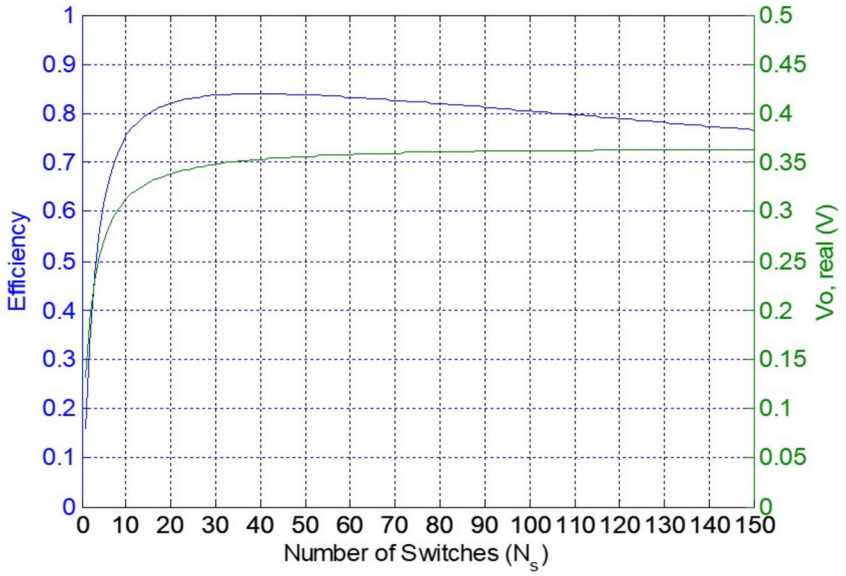

Figure 15. Efficiency and output voltage variation with N_s (switch size) for f_{sw} = 250 MHz and ESR = 0.2 Ω.

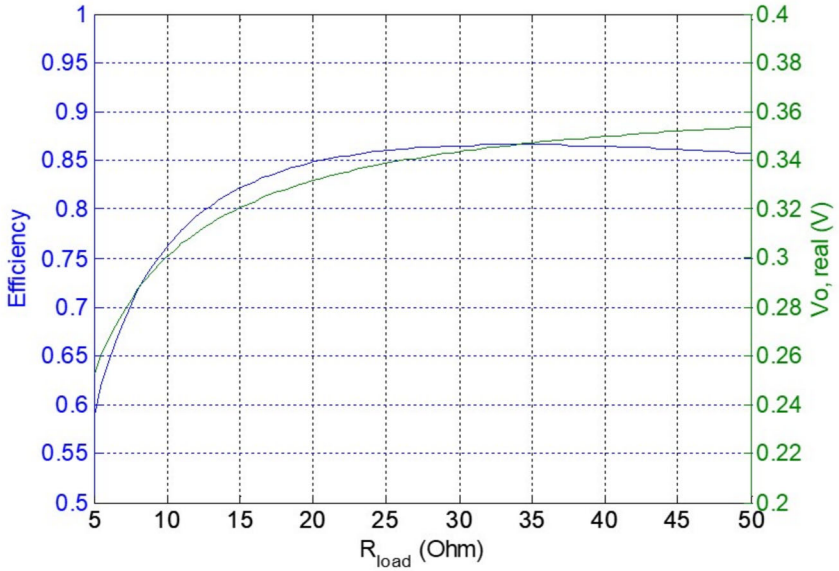

Figure 16. Efficiency and output voltage tradeoff with varying R_{load} for f_{sw} = 250 MHz and N_s = 65 (R_{on} = 0.76 Ω).

Further, a detailed power loss breakdown of the 3:1 Series–parallel SC DC-DC converter is shown in Figure 17. Converter efficiency is affected by these losses, resulting in decreased overall system efficiency. Key insights of these losses are as follows:

- Efficiency is significantly impacted by switching and conductive losses in switches and capacitors. Overall efficiency is increased by lowering these losses. Improving efficiency mostly requires choosing low-ESR capacitors and optimizing switch sizes.
- In this design, bottom-plate capacitor losses and gate drive losses have comparatively less effect on overall efficiency. However, these losses become more important in other topologies or at higher frequencies.

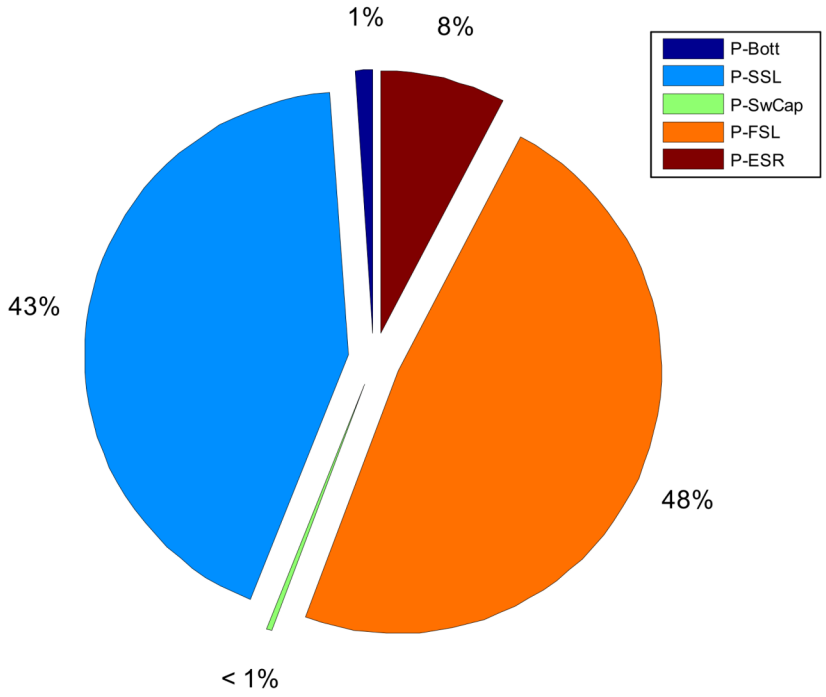

Figure 17. SC converter power-loss breakdown.

Therefore, it is essential to minimize these losses through design choices in order to maximize efficiency. Some examples of these design selections include employing capacitors with lower ESR, choosing components with lower gate charges, and controlling the circuit topology to limit undesired capacitance effects. As demonstrated by Figure 17, this thorough analysis presents an accurate representation of the converter's energy dissipation mechanisms and the loss interpretations that have the most significant impact on efficiency. Further, SC converter efficiency variation with switching frequency and area is shown in Figure 18. The area of the converter depends on the size of the components (switches and capacitors) that are influenced by the switching frequency. As switching frequency increases, the size of passive components (capacitors) decreases, while the switch area may need to increase to handle heat dissipation.

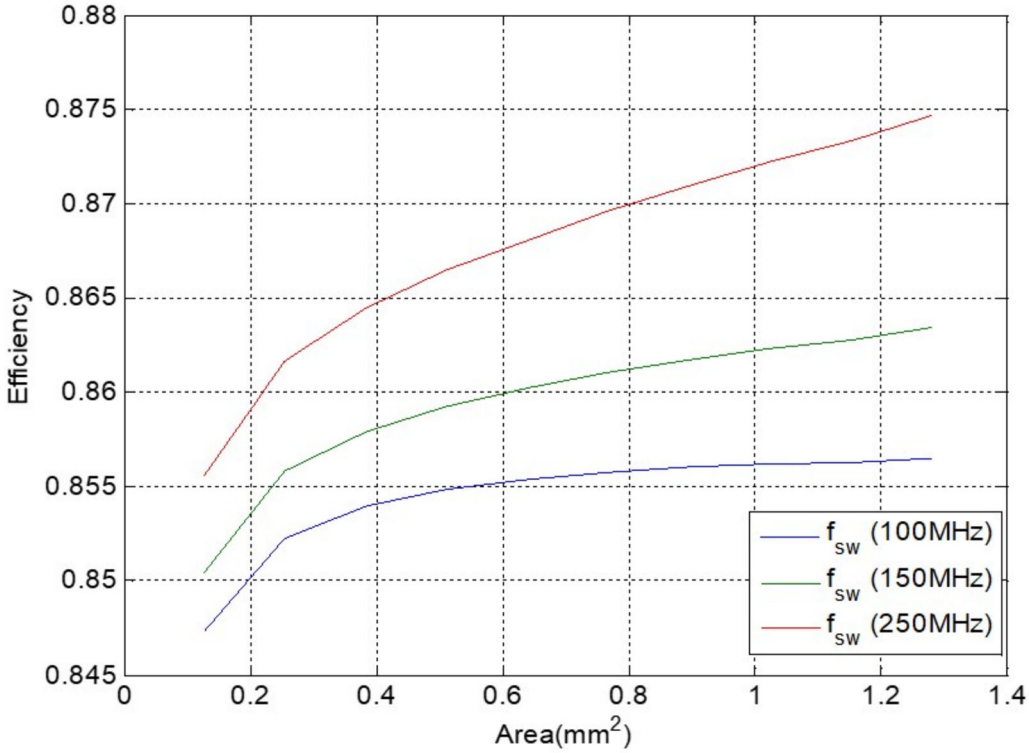

Figure 18. SC converter efficiency variation with switching frequency and area.

This design methodology is relatively robust in terms of scalability for varying power levels, but it does need specific modifications to accommodate significantly changing the load currents or voltage levels. Components that handle larger current and voltage ratings, including switches and capacitors, must be upgraded for higher power applications. For lower power applications, components can be reduced in size, but caution must be utilized to ensure that they still function within safe limits. For varying loads, performance can be optimized by varying the switching frequency. The converter topology can be changed to achieve a variable voltage conversion ratio based on the desired output voltage level. In order to handle greater conversion ratios while maintaining efficiency, consider developing a multi-stage reconfigurable SC converter. The converter architecture can be modified to produce a different voltage conversion ratio. A comparison of the proposed work with the existing literature is presented in Table 3. Peak efficiency, load current, switching frequency, conversion ratio and capacitor technology are some of the performance measures that were compared.

Table 3. The proposed work comparison with the existing literature.

Parameters	[12]	[19]	[20]	[22]	[25]	[26]	[27]	[28]	**Proposed Work**
Result	Simulated	Measured	Measured	Simulated	Simulated	Measured	Simulated	Measured	Simulated
Technology	180 nm	65 nm	250 nm	65 nm	-	0.18 µm	0.18 µm	0.18 µm	22 nm
Capacitor	MOS	Gate oxide	MIM	MOS	Gate oxide	MIM	MIM	MOS	MIM
Gain Ratio	2:1	2:1, 3:1, 3:2	2:1, 5:3, 4:3	2:1	16:1	3:2, 5:3, 2:1, 5:2	2:1	3:1, 2:1	3:1
LoadCurrent	1.5 mA	0.02–5 mA	0.1 mA	138 mA	1 A	2 mA	12 µA–17.8 mA	1.4–5 mA	10 mA
Peak Efficiency	80%	85%	76%	82%	83%	84.2%	80%	74%	86%
Switching Freq.	10 MHz	12 MHz	5 MHz	1 MHz–250 MHz	500 KHz	2 MHz–20 MHz	2 20 KHz–49 MHz	-	250 MHz

In SSL metric comparison, series-parallel topology performs better having larger metric compared to the ladder topology as shown in Figure 19. On the other hand, the performance of the ladder topology is superior at small conversion ratios (nearly equal to 1). For FSL also known as a switch-based metric, the performance of the ladder converter is superior to the series-parallel converter, especially at larger conversion ratios as shown in Figure 20. This is because the high ratio asymptote in the V-A product of switches approaches a constant value in an SC ladder converter. These figures of merits provides a quantifiable measure that reflects the efficiency and power handling capabilities of the active semiconductor and passive components used in the circuit.

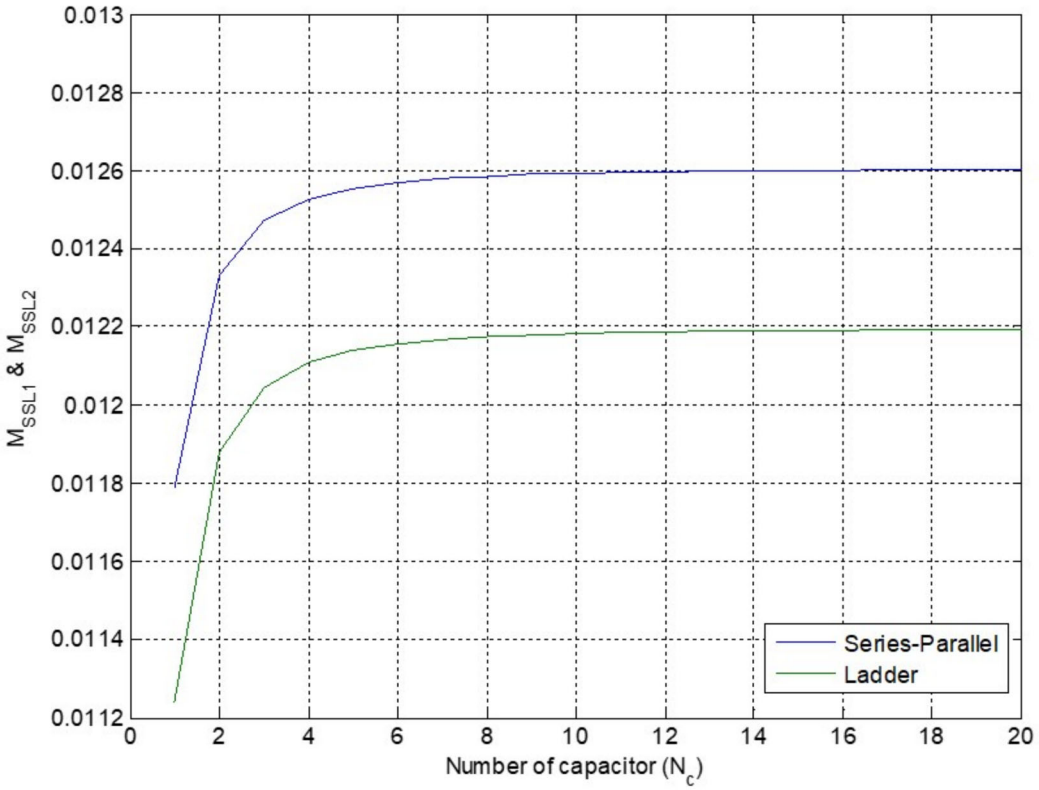

Figure 19. SSL performance matrix (M_{SSL}) comparison of 3:1 Series–parallel/Ladder converters with varying N_C for N_S equal to 65.

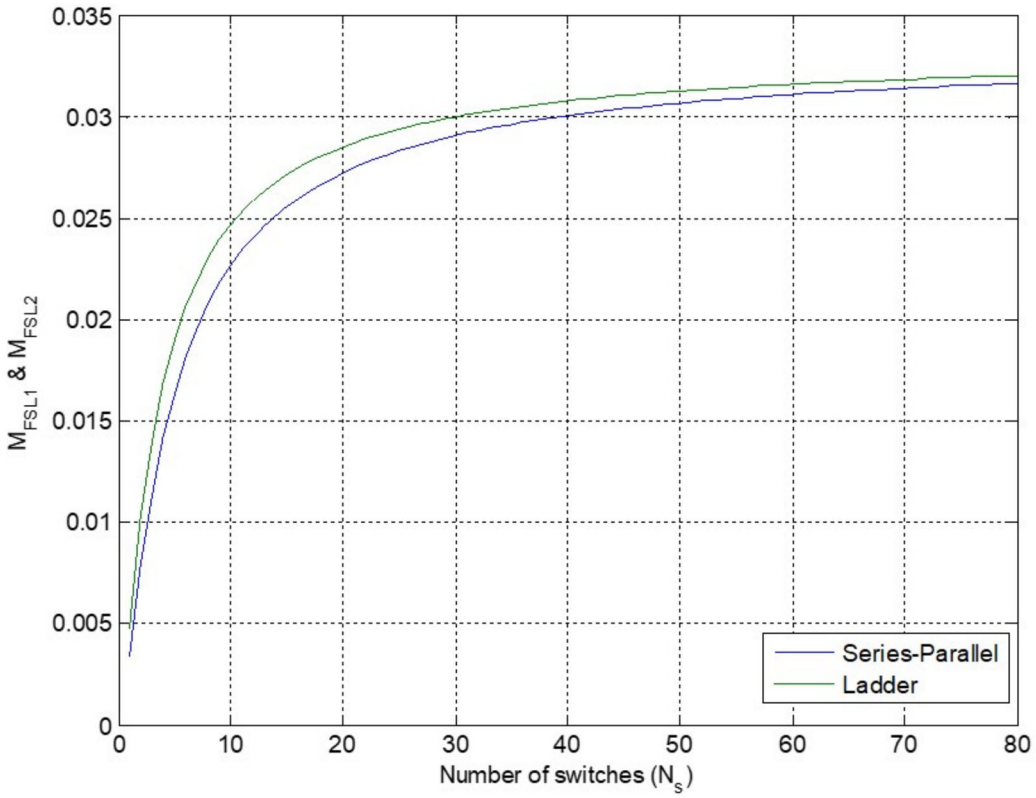

Figure 20. FSL performance matrix (M_{FSL}) comparison of 3:1 Series–parallel/Ladder converters with varying N_S for N_C equal to 20.

6. Conclusions

This study explored the viability of the two types of SC topologies considering both conduction and switching losses for chip-scale power management for PV modules. This work investigates general steady-state performance models and develops minimum attainable performance metrics for SC DC-DC converters, including parasitic. Investigations are conducted on the losses driven by the gate drive, flying capacitor ESR, and the bottom-plate capacitance. To mitigate the losses, the design optimizes both switch size and converter operating frequency to maximize the efficiency of the two-phase 3:1 SC converter for a target load current of 10 mA, implemented in 22 nm process technology. The results shows that in order to achieve the desired efficiency of more than 85% while keeping the minimum output voltage of 0.34 V, a switching frequency of at least 250 MHz is preferred. Further, a topology comparison is performed using performance-limit metrics of output impedance to determine the optimal topology for a specific conversion ratio. The converter with the highest metric will have the lowest output impedance for a given area constraint and conversion ratio. In the SSL comparison, the Series–parallel topology is the most advantageous solution, while in the FSL comparison, the Ladder topology is the most suitable one. Hence, in energy-constrained systems, the Series–parallel topology proved to be the most advantageous topology in terms of the lowest possible power loss. This design methodology enables the optimal design of SC converters for a wide range of applications, such as PV modules, microprocessors, etc. It can further be expandable to reconfigurable multi-phase converters intended for wide output voltage range for low power SoC.

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